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Nickel Silicide as a Contact and Diffusion Barrier for Copper Metallization in Silicon Photovoltaics

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Nickel Silicide as a Contact and Diffusion Barrier for Copper Metallization in Silicon Photovoltaics

By

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Abstract

In this study, NiSi has been formed as the contact for copper front metallization on laboratory silicon solar cells. Transfer length method (TLM) measurements were used to examine the resistive nature of the contact. The scalability of the measurement itself was also examined. Characterization of the NiSi films for thickness, resistivity and composition were performed. Single crystal silicon solar cells were fabricated and used in temperature stress tests of the degradation of the pseudo-fill factor (pFF) and quantum efficiency (QE) to assess the capabilities of the NiSi diffusion barrier. Best contact resistivities of $7.3 \times 10^{-6}\,\Omega\,\mathrm{cm}^2$ with NiSi only and $4.0 \times 10^{-5}\,\Omega\,\mathrm{cm}^2$ with NiSi/Cu/TiN were measured. Even following a week of temperature stress, NiSi maintained solar cell performance parameters such as pseudo fill factor (pFF) and quantum efficiency (QE) better than Cu/TiN contacts without NiSi and at least as good as Ti/Pd/Ag contacts on average.

These methods and materials were applied to high efficiency, textured, solar cells with passivated tunneling contacts. The viability of NiSi in this regime was evaluated by photoluminescence (PL), optical, and TLM measurements. Although the NiSi contact was shown to damage the passivation quality of the contact, a cell capable of an open circuit voltage near 700 mV could be produced using such a contact scheme. Contact resistances as low as $1.8\,\mathrm{m}\Omega\,\mathrm{cm}^2$ were formed, as compared with industry standard screen printed Ag contacts which form best contact resistivities in the range of $1.5\,\mathrm{m}\Omega\,\mathrm{cm}^2$.

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Chapter 1

Introduction and Motivation

The photovoltaics industry has seen massive growth in the past decade. Since 2005 the annually installed capacity of photovoltaics (PV) has grown over 2700%.[1] One of the main forces behind this growth is the unprecedented decrease in price per Watt of PV power. As such, competition for market share and the motive to reduce production costs are at an all time high. Due to this growth, PV is no longer an insignificant portion of the world's energy production. Last year in the U.S. PV represented 36% of all new electric capacity added.[2]

As shown in Figure 1.1, the median reported PV system cost has decreased at an average of approximately 7% per year since 1998, and at an even greater rate since 2009.[3] Due to the rapid market growth and dropping prices, competition for market share and the will to reduce production costs are at an all time high.

Silicon PV represents 90% of the industry. This is illustrated in Figure 1.2. Aside from the cost of the wafer, the silver front metallization is the largest single cost factor, representing more than 7% of the cost of goods sold, or nearly 50% of the cost of the cell itself.[4] This cost has driven manufacturers to continue to reduce the quantity of silver used in the cell. The International Technology Roadmap for Photovoltaics (ITRPV)[5] has estimated the reduction of silver content in a cell to reach 0.03 g/cell

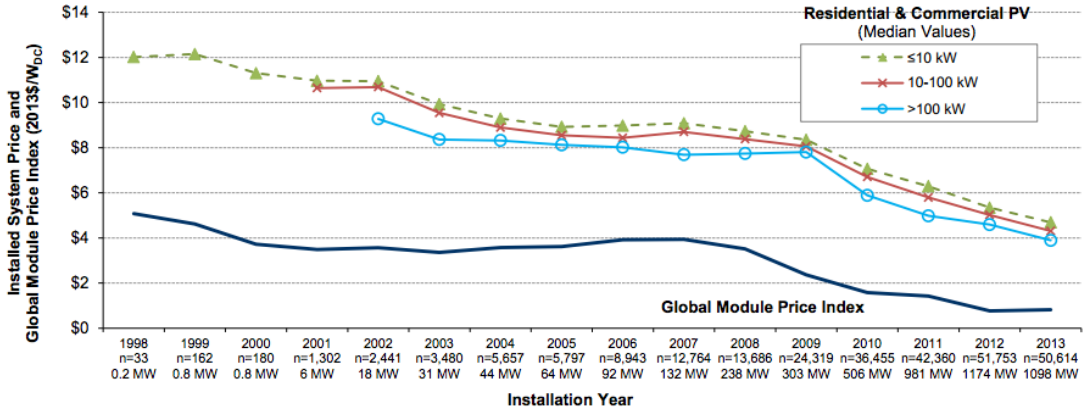


Figure 1.1: The reported drop in price of installed PV systems.[3]

by 2024, as shown in Figure 1.3. Various advanced deposition techniques such as double printing have been investigated in industry in pursuit of this. Additionally, the trend in reduction of wafer thickness is also expected to continue. This poses another problem for silver metallization.

Currently in industry, silver is typically deposited on a cell via screen printing. Screen printing utilizes a metal screen with openings positioned appropriately for the cell's gridlines. The screen is filled with silver paste and as this occurs the screen is forced into contact with the wafer by a squeegee and the paste is pushed through the openings onto the wafer. The paste, containing glass frit, is then fired. The paste reacts with the silicon nitride antireflection coating (ARC) and contact to the silicon is made. Best contact resistivities in in the range of $1.5\,\mathrm{m\Omega\,cm^2}$ have been produced using this method.[6]. Since this printing process requires hard contact to the wafer, thinner wafers will not withstand this processing and thus an alternative technology will be required; inkjet printing, aerosol jet printing, and plating technologies are the strong potential candidates. In addition to the aforementioned impediments to

silver's dominance as the preferred PV front metallization technology, the price of silver has increased dramatically in recent years as exhibited in Figure 1.4.

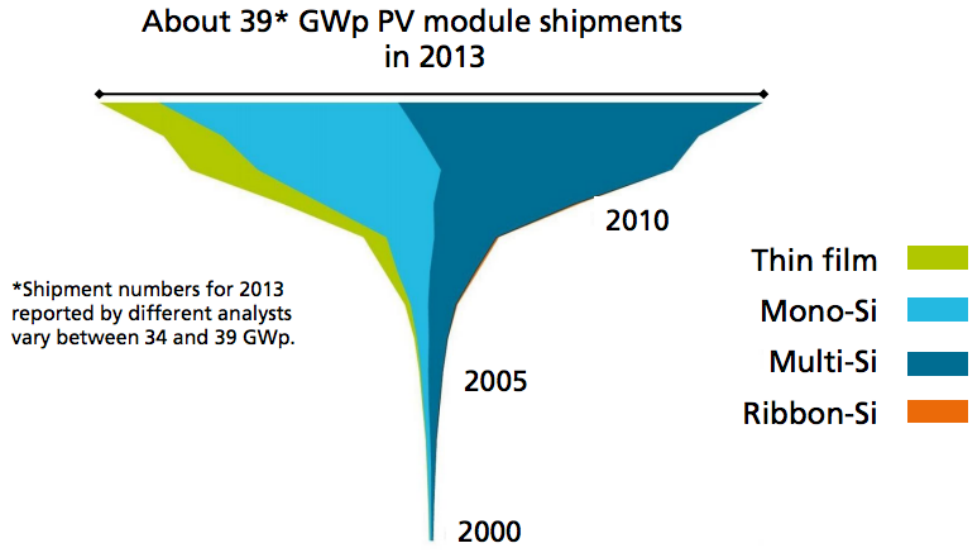


Figure 1.2: The shipped capacity of PV modules since 2000.[7]

Copper presents a viable and sustainable alternative to silver with the potential to reduce metallization costs by approximately 50% as illustrated by Figures 1.4 and 1.5 while maintaining device performance in preliminary investigations. This is largely due to the low resistivity of copper, outperformed only by silver, and by less than 4%. The room temperature resistivity of a few metals relevant in silicon PV are shown in Figure 1.5.

While there are significant advantages to the implementation of copper metallization in photovoltaics, there are still significant obstacles to be overcome. Copper oxidizes at very low temperature and thus a capping layer such as tin must be used. If a capping layer is not used, the resistance of the copper will increase dramatically

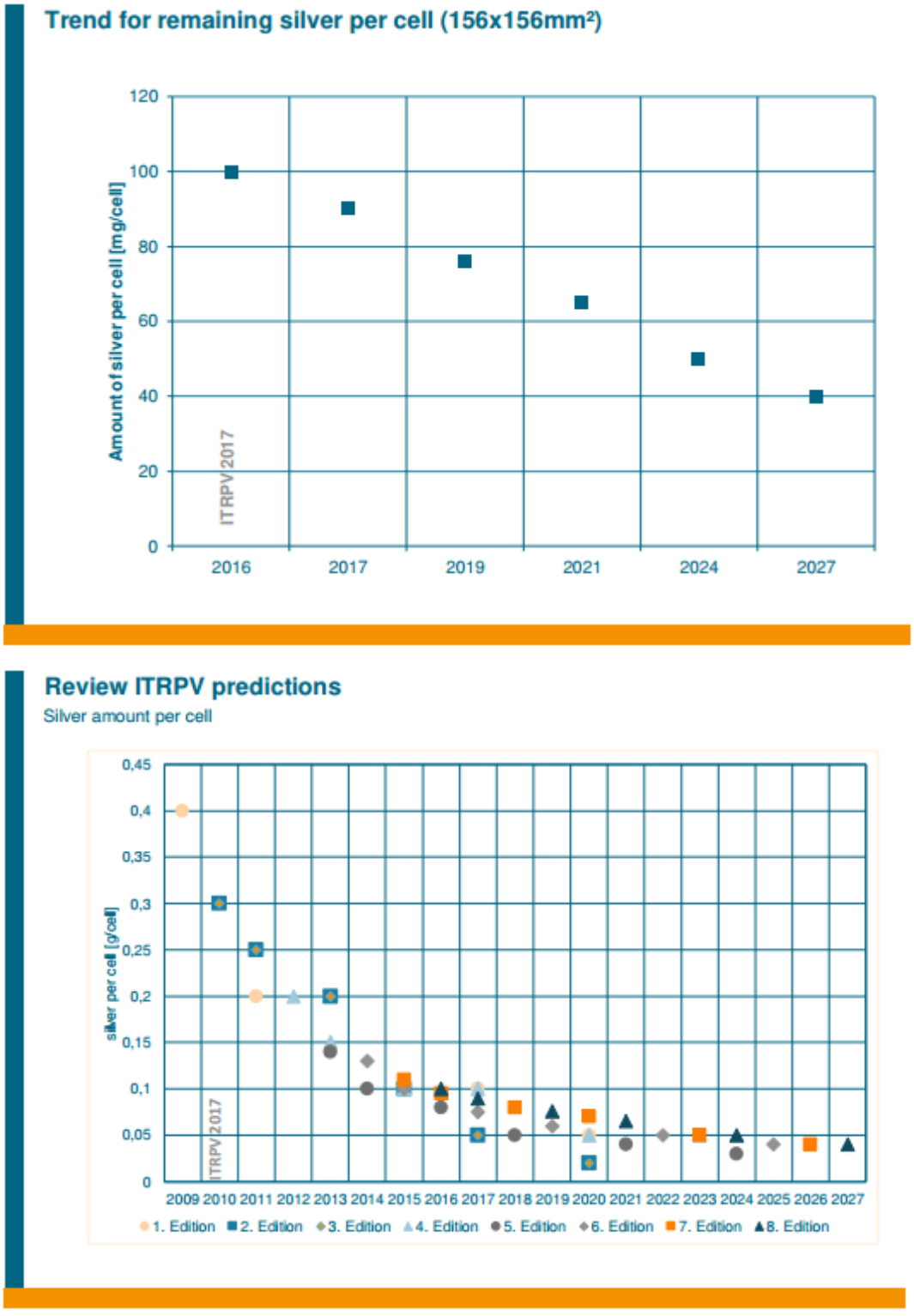
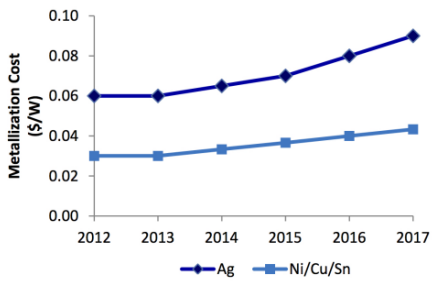


Figure 1.3: The predicted reduction in silver content per cell.[5]

Figure 1.4: The price of silver and copper since 2007.[8]



Metal	Resistivity (μΩ-cm)
Ag	1.63
Al	2.82
Cu	1.69
Ni	7.19
Sn	10.9

Figure 1.5: Metallization cost comparison between silver and a Ni/Cu/Sn scheme.[4]

as is oxidizes. Fortunately, tin plating technologies are well established. Plating copper itself is also a well established technology and is used extensively in back end of line (BEOL) processing of integrated circuits (IC). These benefits, as well as the promising early results from attempts at copper screen and inkjet printing give even more impetus to copper as the primary front metal in PV. The primary concern with copper is due to its quick diffusion in silicon where it acts as a deep level trap, greatly diminishing the efficiency of the device. To prevent this, a diffusion barrier layer is needed. Nickel has shown to be an effective copper diffusion barrier in silicon solar cells.[9][6] The diffusivity of copper, nickel, and silver are shown in Figure 1.6. Issues due to large electrical contact resistance and adhesion issues in a Ni/Cu/Sn metallization scheme have given cause for silicidation at the Ni/Cu interface to produce nickel monosilicide (NiSi). Nickel monosilicide is the Ni/Si phase of choice as it is the lowest resistivity phase, has low contact resistance to silicon, forms at fairly low temperatures, consumes a fairly small amount of silicon, and has been used extensively in the IC industry. In the NiSi/Ni/Cu/Sn scheme, a thin nickel layer is printed on the cell. It is then annealed to produce NiSi. Following this, a thicker nickel layer can be plated to ensure minimal diffusion of copper. Copper and tin are then plated, one after the other. The long term reliability and full commercialization of this metallization scheme has not been fully explored, but results from several groups show it to be very promising. The aim of this work is to investigate and optimize a NiSi film as the sole diffusion barrier and contact to copper. The potential of this arrangement is due to the added processing simplicity, material cost savings, and added series resistance due to the fairly high resistivity of nickel.

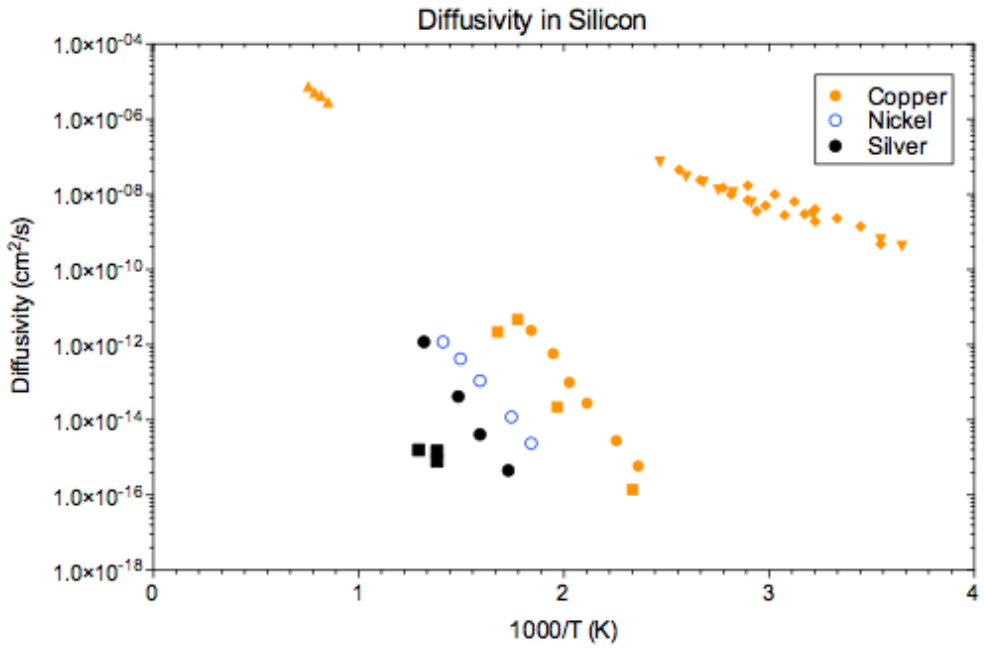


Figure 1.6: Diffusivity of Cu, Ni, and Ag in Si. Data compiled by Fisher.[10]

In this study, supported under the U.S. Department of Energy's, Sunshot Incubator Award program, NiSi was formed as the contact for copper front metallization on laboratory silicon solar cells, fabricated at the Rochester Institute of Technology (RIT). Transfer length method (TLM) measurements are being used to examine the resistive nature of the contact. The scalability of the measurement itself has also been examined. Characterization of the NiSi films for thickness, monitored by X-ray reflectometry (XRR) and transmission electron microscopy (TEM), and composition, via Auger Spectroscopy and X-ray diffractometry (XRD), has been performed. Baseline, rapid prototyping, c-Si solar cells have been fabricated using a tailored version of RIT's turnkey solar cell process.[11][12] These cells were used in a temperature stress test of the degradation of the pseudo-fill factor (pFF) and quantum efficiency (QE)

to assess the capabilities of the NiSi diffusion barrier. Properties of a NiSi film were modified to maintain low contact resistance and also sufficiently retard the diffusion of copper.

These methods and materials were applied to high efficiency, textured, solar cells with passivated tunneling contacts provided in collaboration with the National Renewable Energy Laboratory. The viability of NiSi in this regime was evaluated by photoluminescence (PL), optical, and TLM measurements.

Chapter 2

Literature and Background

2.1 Solar Cell Operation

Carriers in a solar cell are typically collected by means of a simple p-n junction. The traditional structure of c-Si solar cells favors a thin n-type layer, called the emitter and a thick p-type layer, called the base. When a p-type semiconductor layer is in contact with an n-type semiconductor layer majority carriers of each will diffuse into the other. When this occurs, fixed, ionized donor and acceptor atoms are left behind. As the diffusion continues a built-in electric field is formed at the junction between the layers. The current associated with this field is called the drift current. The force associated with this field opposes the diffusion of carriers and equilibrium between the two is reached. The region around the junction that contains this electric field is known as the depletion, or space charge, region (SCR) since the electric field sweeps charged carriers out of this region.

When photons are absorbed in a semiconductor electron-hole pairs are created, as shown in Figure 2.2. The electron is excited to the conduction band and, by this action, a hole is created in the valence band. For this to occur, the energy of the absorbed photon must be greater than or equal to the energy band gap, E_g between the valence and conduction bands. A solar cell operates under the low-level

injection (LLI) condition in which the generation rate of carriers is much less than the doping of the semiconductor. This means that upon illumination, the relative concentration of minority carriers is greatly increased whereas the relative majority carrier concentration is not. This makes solar cells minority carrier devices.

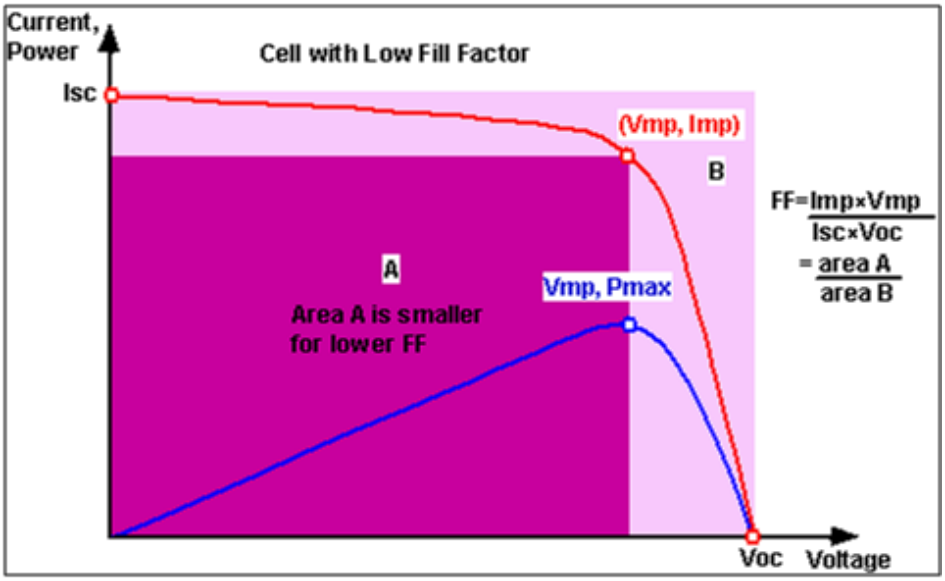


Figure 2.1: The I-V curve of a typical solar cell.[13]

If minority carriers generated by the light reach the SCR, they are swept across to the other side via the built in electric field. This means the drift current is increased under illumination, since there are many more minority carriers present which can be swept across the junction, unlike the majority carriers which are kept on their respective sides by the electric field of the SCR. Under open circuit conditions, the carriers build up on either side. This build up of charge increases the diffusion current since the concentration gradient has increased. These two currents exactly balance each other in an open circuit and the separation of charge creates the open circuit voltage, V_{oc}. Under short circuit conditions, this equilibrium is disturbed since no

build up of charge can occur. This reduction in carrier concentration gradient reduces the diffusion current, allowing the drift current to dominate, providing a net current, short circuit current, I_{sc}.

A typical solar cell I-V curve of a solar cell is shown in Figure 2.1. To operate a solar cell at the point of maximum power generation, an appropriate load resistance is needed. Since I_{sc} and V_{oc} are respectively the maximum current and voltage possible for the cell, it would be ideal to have an I-V curve as "square" as possible. This "squareness" is characterized by the fill factor, FF, as shown in Figure 2.1

2.1.1 Recombination

Charge carriers will simply recombine back to their lower energy bands if there is no mechanism to collect and send them through an external circuit. This recombination is known as band to band, or radiative recombination due to the emission of a photon of energy equal to the energy lost by the carrier in transition.

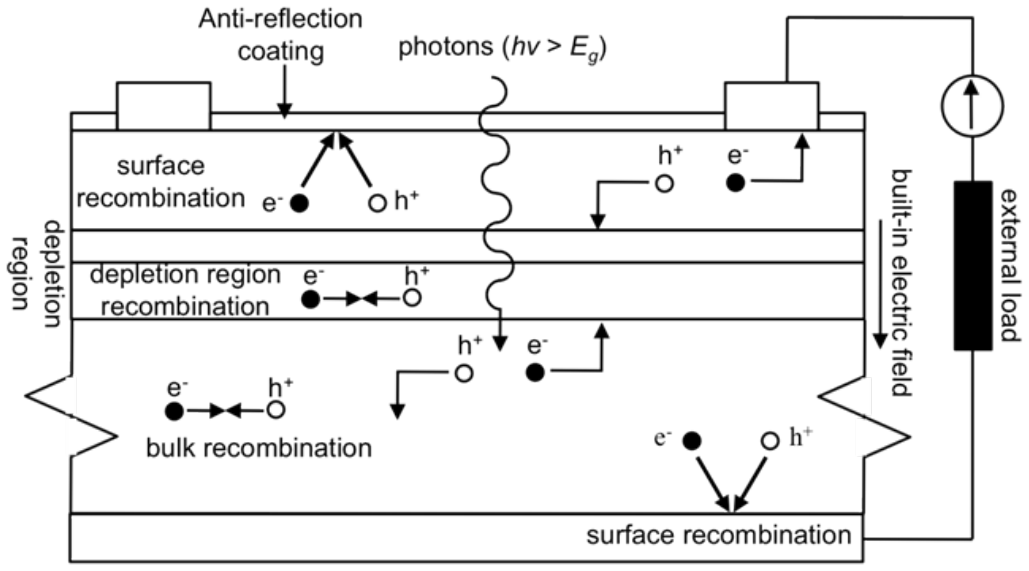


Figure 2.2: The movement of charge carriers in a typical solar cell.[14]

A second recombination mechanism is defect assisted recombination also known as Shockley-Read-Hall (SRH) recombination, as the process is described by SRH statistics. In this form of recombination a defect, or trap, creates an energy state in the otherwise forbidden energy gap between the conduction and valence bands. If a carrier enters this state it can be trapped there until it is thermally excited out of the trap. If a carrier of the opposite type is excited to this state before the first one can leave, recombination occurs and the energy used to excite these carriers is wasted. If the trap energy state is located near the center of the band gap, it is known as a deep level trap. These are the most effective trap levels for recombination. This is because trap states near either band are more likely to allow the carriers to be thermally excited out of the trap. This type of recombination is more important in indirect band gap semiconductors, like silicon. This is because the defect allows for transfer of momentum as well as energy. Direct band gap semiconductors in which the transfer of momentum to the crystal lattice is not necessary primarily exhibit radiative recombination.

The third type of recombination is Auger recombination. In this scenario three carriers are involved. An example of this could be between two conduction band electrons and one valence band hole. Energy and momentum can be transferred from one conduction band electron to the other. The electron then drops to the valence band and eliminates a hole. The excited second electron then thermally relaxes back to the bottom of the conduction band. Since a third carrier is required, Auger recombination is most relevant in regions of high carrier concentration, which presents a limit to the range of effective dopant concentrations.[15] The LLI condition

also keeps Auger combination at a relative lower level also due to a reduction in excess carrier concentration.

From these phenomena the bulk minority carrier diffusion lifetime, τ_{Bulk} can be defined. This parameter describes how long a free carrier can diffuse in the cell before it recombines. Paired with the diffusivity of the material, the minority carrier diffusion length can be determined. It can be described as a combination of the lifetime resulting from each recombination mechanism as represented in Equation 2.1.

$$\frac{1}{\tau_{Bulk}} = \frac{1}{\tau_{Rad.}} + \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{SRH}} \tag{2.1}$$

Surface recombination velocity is another metric of recombination; it quantifies the rate at which carriers recombine at the imperfect crystal structure at the material surface. The surface recombination velocities can be combined with the bulk recombination rates to define an effective minority carrier lifetime.

These values are very important in determining the potential power output of a solar cell. For optimal performance, the lifetime should be as long as possible, but it is essential that the diffusion length is long enough such that carriers can at least reach the junction so that they can be collected by the circuit.

2.1.2 Impurities in Silicon Solar Cells

Impurities in silicon behave differently depending on the way they interact with the silicon lattice and the energy state they create as a defect. The defect levels of several impurities are shown in Figure 2.3. Given the diffusivity and trap levels of each, Cu posses the greater threat as it can accumulate in great concentrations throughout

the bulk while the Ni is more likely to be limited to the emitter where lifetimes are already low.[10]

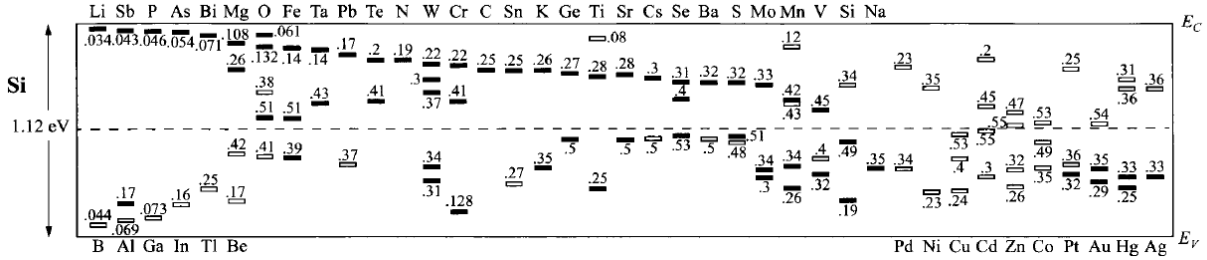


Figure 2.3: The trap levels of several impurities. Below mid-gap they are measured from E_V and above mid-gap they are measured from E_C.[16]

In essence Cu must be prevented from entering the cell or it will relatively quickly reach higher concentrations in the base as well as degrading the junction; whereas the diffusivity of Ni keeps it from reaching high concentrations anywhere too far from the contact on the emitter, where the carrier lifetime is already short. It has been shown in real devices that balance of the risks of the two materials favors Ni as the immediate contact, as is discussed in the later sections.

2.1.3 Electrical Resistance in Solar Cells

The resistances associated with any electrical device are critical in determining its performance. The parasitic, internal, resistive nature of a device can be characterized by its parallel, or shunt, resistance and its series resistance. The shunt resistance is in parallel with the light generated current and provides a path for the current other than through the load where useful power is extracted. The resistance in series with the current source allows power to be dissipated in a non-useful manner since a voltage drop across the internal resistance detracts from the voltage available across

the load.

In a solar cell the series resistance is a critical concern. Each element, or component, of the solar cell structure carries its own contribution to the total series resistance. The major contributing elements are outlined in Figure 2.4, and from the back of the cell to the front these are the resistance of the back metal contact, the base, the emitter, the front metal contact, the fingers and the busbars. These resistances are dependent on the bulk resistivities of the particular material, the dimensions of that element and the density and manner in which current flows through that element. While the resistance in the bulk is straightforward, the resistances associated with the metal-semiconductor junctions, or contact resistances, are more complicated. Due to the small area of contact on the solar cell front, the resistance associated with the front metal contact is significant because of the increased current density. Contact resistance is often discussed in terms of the contact resistivity, ρ_c, defined in Equation 2.2. This allows for convenient comparison of different sized contacts.

$$\rho_c = \left.\frac{\partial V}{\partial J}\right|_{V=0} \tag{2.2}$$

The Schottky model allows for three types of metal-semiconductor (MS) junctions depending on the work function of the metal (ϕ_M) with respect to the work function of the semiconductor (ϕ_S). These are shown in Figure 2.5 for $\phi_M < \phi_S$, $\phi_M = \phi_S$, and $\phi_M > \phi_S$ respectively. The accumulation type junction is the preferred junction for an ohmic contact as the barrier to current flow is the smallest. In an ideal case

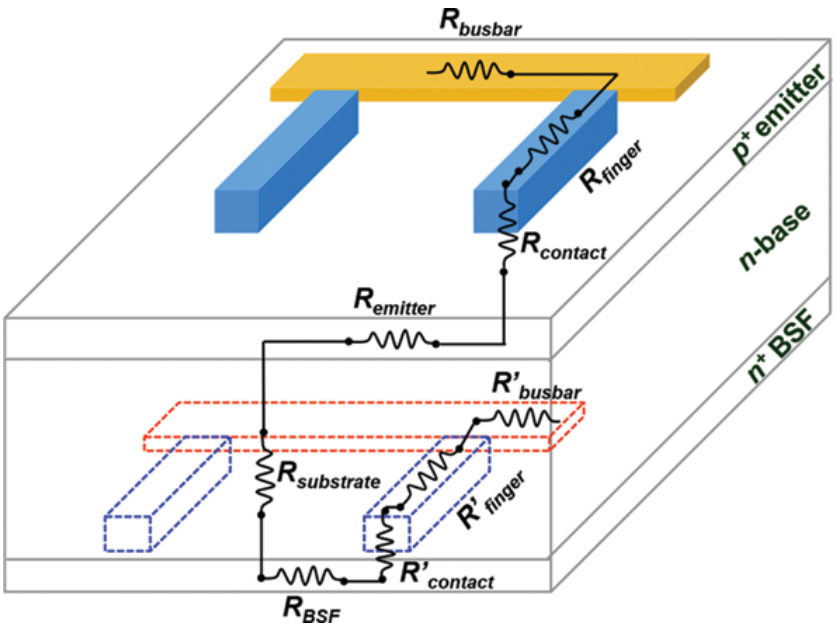


Figure 2.4: The various major components of a solar cell contributing to series resistance.[17]

a metal work function could be chosen to achieve this type of junction. However, this type of junction is not practically realized in actual devices.[] In a real device the Fermi level is pinned by semiconductor surface states and a depletion type barrier is formed independent of the metal work function.[18]

In a depletion type MS junction, current across the barrier can be grouped into three types: thermionic emission (TE), thermionic/field emission (TFE), and field emission (FE). These are shown in Figure 2.6. With TE the carrier is thermally excited over the energy barrier. In FE the carrier tunnels through the barrier. In TFE a combination of TE and FE occurs. Due to the pseudo-triangular shape of the barrier, it is easier for carriers to tunnel at higher energies where the barrier is narrower. The share each type of emission holds is dependent on the barrier width, which is strongly dependent on the dopant concentration in the semiconductor. At

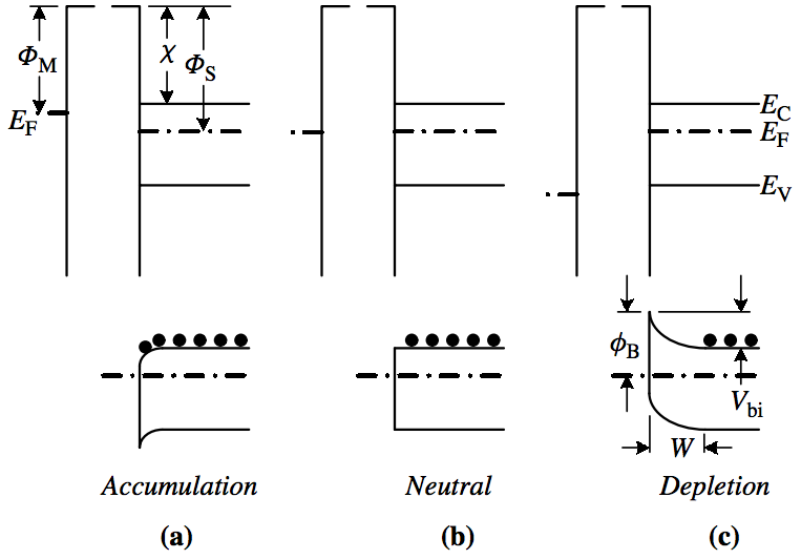


Figure 2.5: The three metal-semiconductor junction types before and after the contact has formed.[18]

higher dopant concentrations ($>10^{19}\,\mathrm{cm}^{-3}$) FE begins to dominate since the barrier is narrow and carriers can more easily tunnel through it./citeSchroder This is the regime in which a typical silicon solar cell operates since the surface of the emitter is highly doped. In some technologies the area under the metal is intentionally doped even higher to improve the FE tunneling current.

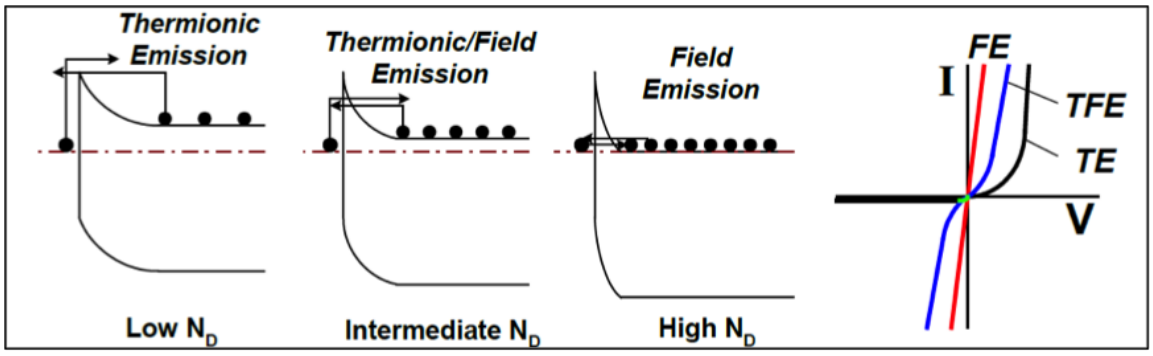


Figure 2.6: The three mechanisms allowing current flow across an MS depletion barrier.[18]

The actual contact resistivity deviates from this value due to non-idealities such as effects from current crowding, spreading resistance, interfacial oxides and resistance in portions of the semiconductor and metal near the interface that are affected by the contacting process and nature of the interface.

2.2 Measurement Techniques

2.2.1 Transfer Length Method (TLM)

Dissipation of power over a series resistance is one of the leading efficiency limiting mechanisms in a solar cell. One of the primary sources of series resistance is contact resistivity. A contact resistivity larger than $2\,\mathrm{m\Omega\,cm^2}$ represents a 5% or greater loss in power due to series resistance.[19]

The leading measurement method for contact resistivity is by the Transfer Length Method (TLM) as it allows for the contact resistance, contact resistivity (area normalized) and sheet resistance under the contact to be easily measured. A typical TLM structure is shown in Figure 2.7.

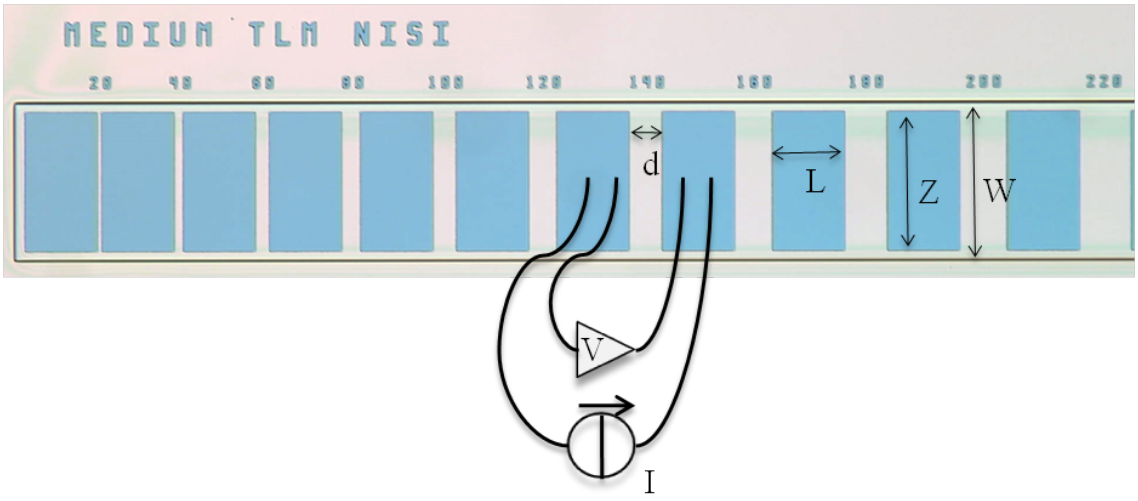


Figure 2.7: A typical TLM structure with labelled dimensions.

TLM structures consist of metallized pads separated by spacings of various sizes atop a mesa or diffusion of width, W. The resistance between each pad can be measured and plotted as illustrated in Figure 2.8.

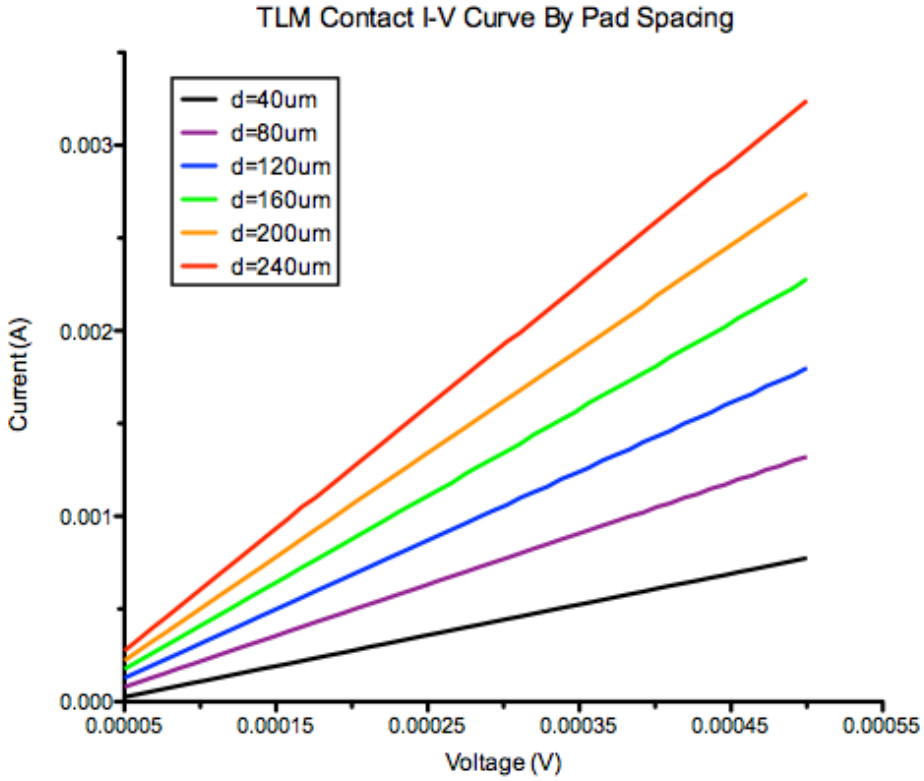


Figure 2.8: The current-voltage characteristic across increasingly distanced metal pads on a mesa with emitter diffusion.

The resistance between TLM pads as a function of pad spacing is shown in Figure 2.9 and expressed in Equation 2.3. The contact resistivity (rho_c) and sheet resistance (ρ_s) of a diffused layer can be extracted from the slope and intercepts of such a plot, given the relationships in Equations 2.3-2.6. See Figure 2.7 and 2.9 for definitions of the parameters used in the following equations.

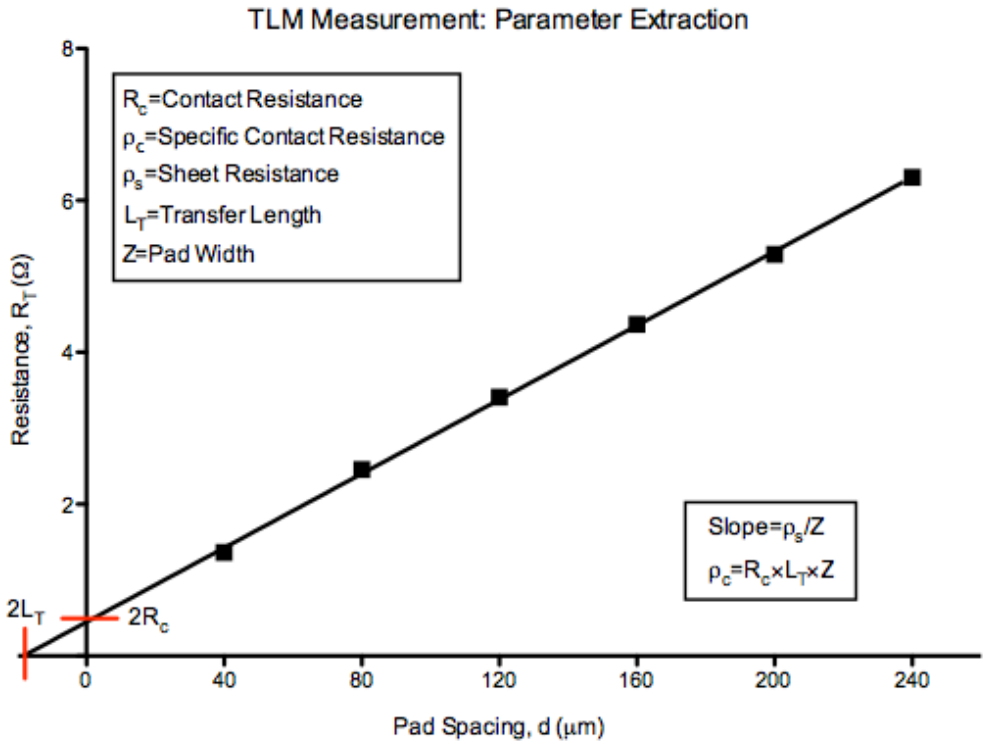


Figure 2.9: The resistance between TLM pads as a function of pad spacing.

$$R_T = \frac{\rho_s d}{Z} + 2\frac{\rho_c}{L_T Z} \tag{2.3}$$

Given the typical conditions of a solar cell, resistance of the contact is given by Equation 2.4 and the transfer length is given by Equation 2.5.[18] Physically, the transfer length is the length over which current is transferred in the contact, as defined by the "1/e" point of the voltage distribution over the contact.[18]

$$R_c = \frac{\rho_c}{L_T Z} \coth\left(\frac{L}{L_T}\right) \tag{2.4}$$

$$L_T = \sqrt{\frac{\rho_c}{\rho_s}} \tag{2.5}$$

The metal resistivity is assumed to be zero in this case. This is not an accurate assumption for silicided contacts, adding the following complication of Equations 2.6, where ρ_m is the sheet resistance of the metal or silicide and L'_T is the corrected transfer length given this complication[18].

$$R_c = \frac{L'_T}{Z}\left\{\frac{({\rho_m}^2 + {\rho_s}^2)}{(\rho_m + \rho_s)}\coth(L/L'_T) + \frac{\rho_m \rho_s}{(\rho_m + \rho_s)}\left[\frac{2}{\sinh(L/L'_T)} + \frac{L}{L'_T}\right]\right\} \tag{2.6}$$

$$\text{where } L'_T = \sqrt{\frac{\rho_c}{(\rho_m + \rho_s)}} \tag{2.7}$$

2.2.2 Quantum Efficiency (QE)

Ideally, each photon incident upon a solar cell will create an electron hole pair and current will be derived from the generated charge carrier. However, in a realistic device, this does not occur for several reasons. The first such reason is that not every

photon incident on a solar cell will be absorbed by the cell. Some photons will be reflected and some will be transmitted through the cell. This is highly dependent on the wavelength of the photon (λ) as different energy photons are characteristically absorbed at different depths in a given material, depending on the extinction coefficient of the material (k). The intensity of light (I) is represented by Equation 2.8 for any depth (z), depending on the incident intensity (I_0). At the absorption depth (δ), given in Equation 2.9, 1/e of the light has been absorbed.

$$I = I_0 \mathrm{e}^{\alpha z} \tag{2.8}$$

$$\delta = \frac{1}{\alpha} = \frac{4\pi k}{\lambda} \tag{2.9}$$

Not every carrier that is generated can be collected, due to the various recombination mechanisms. The quantum efficiency is a measure of how effectively light is converted to current. Since light of different wavelengths is characteristically absorbed at different depths, the quantum efficiency of the cell varies with the wavelength because different areas of a cell display different recombination effects. The external quantum efficiency of a typical silicon solar cell is shown in Figure 2.10. The internal (I.Q.E.) and external quantum efficiencies (E.Q.E.) are defined below in Equations 2.10 and 2.11.

$$\text{E.Q.E.} = \frac{\text{Electrons Collected}}{\text{Photons Incident}} \tag{2.10}$$

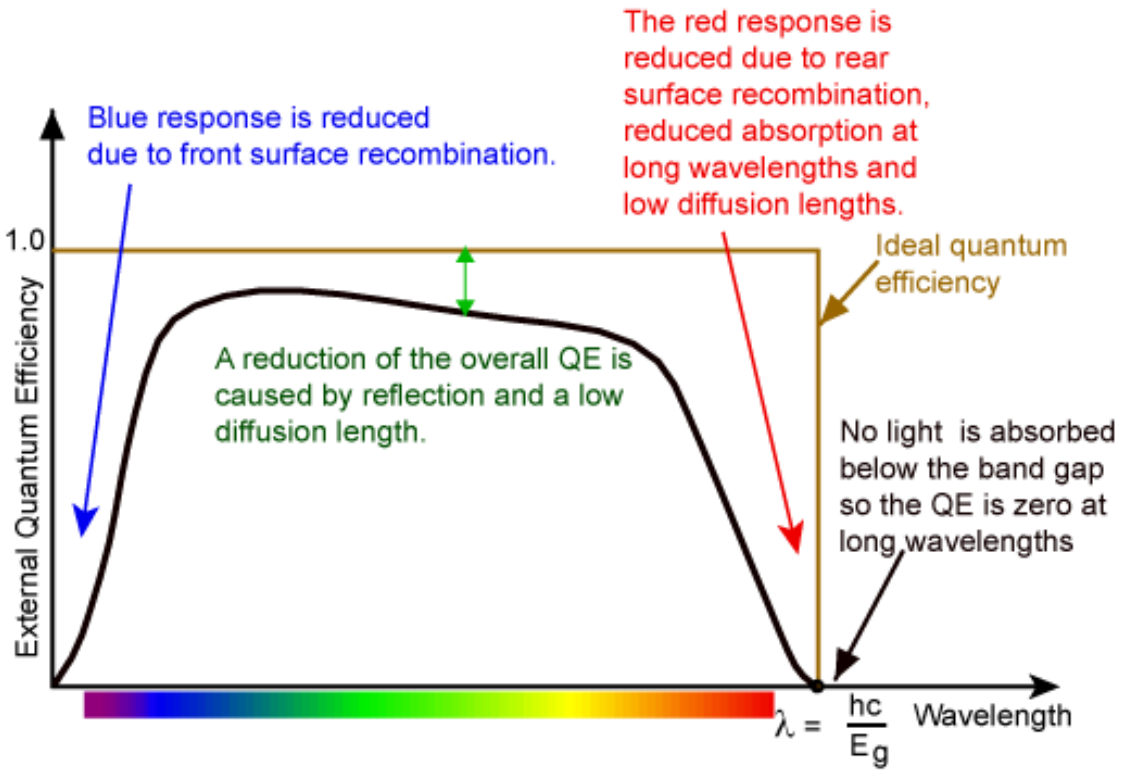


Figure 2.10: The quantum efficiency of a typical silicon solar cell.[13]

$$\text{I.Q.E.} = \frac{\text{Electrons Collected}}{\text{Photons Absorbed}} \tag{2.11}$$

$$= (1 - R)\text{E.Q.E.} \tag{2.12}$$

Quantum efficiency cannot be measured directly. Instead, the I_{SC} is measured at discrete wavelengths where the total incident power of the beam is known. The ratio of these quantities is defined as spectral response (S.R.). This is related to quantum efficiency as shown in Equation 2.13.

$$\text{S.R.} = \frac{I_{SC}}{P_{In}} = \frac{q\lambda}{hc}\text{E.Q.E.} \tag{2.13}$$

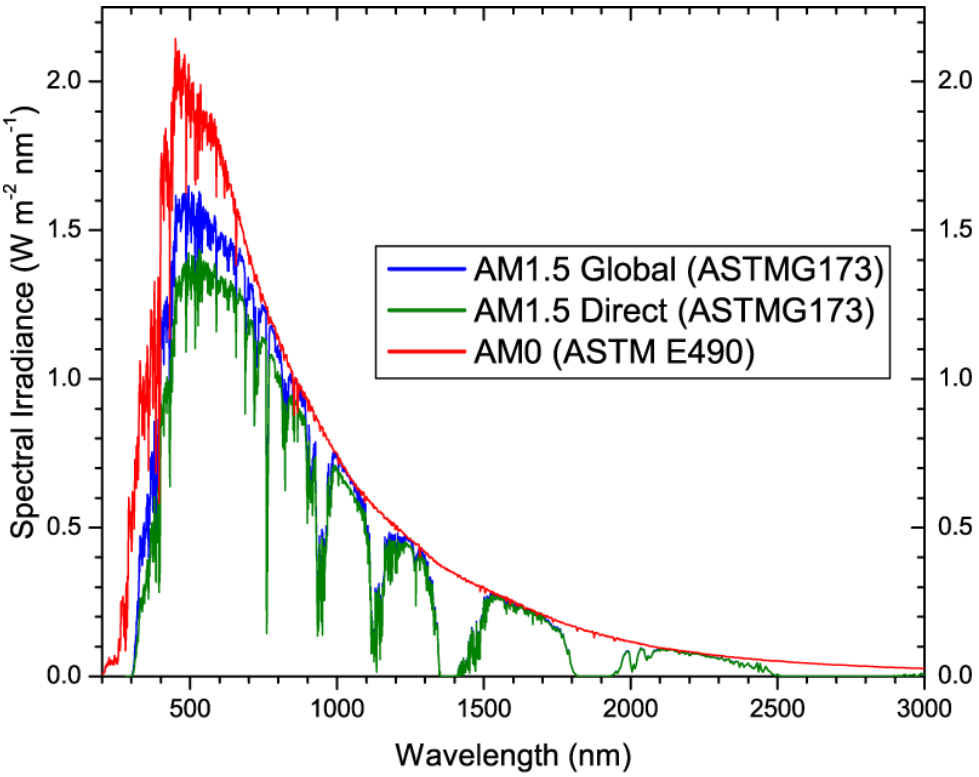


Figure 2.11: The quantum efficiency of a typical silicon solar cell.[13]

Quantum efficiency is an excellent method for diagnosing performance issues with a solar cell since it gives spatial information. However, it is important to note that not all wavelengths are as critical to the power efficiency of the cell.

Air mass (AM) is defined by the ratio of the optical path length to the sun to the optical path length of the sun if directly overhead. Over the period of a day the sun moves through a range of angles in the sky. This affects the amount of atmosphere the incident light travels through, and therefore the air mass. The change in solar angle creates spectral variations due to the change in air mass and a change in diffuse scattered light from the atmosphere. The AM0 and AM1.5 standard solar spectra are shown in Figure 2.11, where AM0 is the extraterrestrial spectrum, AM1 (not shown) represents the spectrum if the sun was directly overhead, and AM1.5 is the standard spectrum used to represent conditions in the northern hemisphere, defined at a lattitude of 48.2°. To achieve the best performance, a solar cell must have an adequate quantum efficiency for the wavelengths which are most abundant in the spectrum of interest.

2.2.3 Photoluminescence (PL) and Implied V_{oc}

Photoluminescence (PL) measurements can be made by exciting carriers in a semiconductor using a laser. If these carriers relax via band to band, radiative, recombination the emission of light can be captured with a camera, giving a spatially resolved image, over the front area of a sample, of recombination in the semiconductor. If carriers relax via trap assisted SRH recombination, the wavelength of emitted light will be characteristically different. A filter and the correct detector can be used to tune

the desired wavelength range, as shown in Figure 2.12, so that a relative comparison of radiate recombination can be made. Si PL has a wider distribution of emitted wavelength as an indirect bandgap semiconductor. This PL technique is similar to electroluminescence measurements performed by externally powering a solar cell and capturing the emission of light. Photoluminescence is convenient for in-line measurement since it does not require a fully processed or metallized cell.

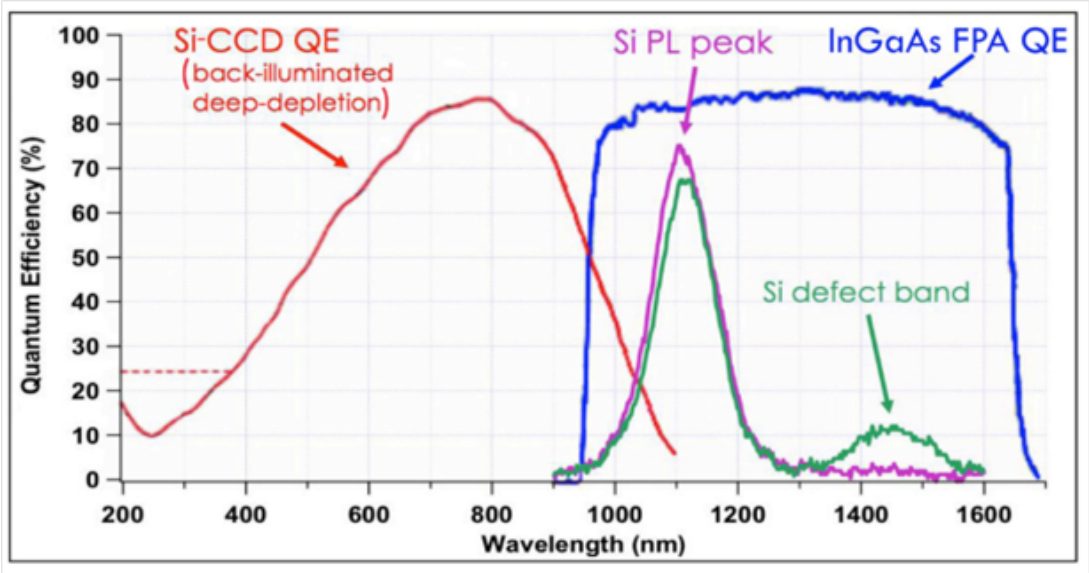


Figure 2.12: The quantum efficiency of a photodetectors used in PL measurements and typical Si PL emission spectrum.[20]

When the open circuit voltage is determined from carrier concentration [21] it is referred to as the implied open circuit voltage (iV_{oc}). This is expressed below in Equation 2.14

$$iV_{oc} = \frac{kT}{q} \ln\left(\frac{(N_A + \Delta n)\Delta n}{{n_i}^2}\right) \tag{2.14}$$

where kT/q is the thermal voltage, N_A is the doping concentration, Δn is the excess

carrier concentration and n_i is the intrinsic carrier concentration.

The difference in iV_{oc} between two regions in a PL image can be calculated as shown in Equation 2.15

$$\Delta iV_{oc} = \frac{kT}{q} \ln\left(\frac{PL_1}{PL_2}\right) \tag{2.15}$$

where PL_1 and PL_2 are the PL intensities from regions 1, and 2 respectively. This is possible since the difference in intensity is related to a difference in excess carrier concentration.[22]

2.2.4 Suns-V_{oc}

In the suns-V_{oc} method, the open-circuit voltage, V_{oc}, is measured as the illumination incident on the cell is increased. At each level of illumination, the short circuit current, J_{sc} is measured on a reference cell. A similar method is often used in which J_{sc} and V_{oc} are both measured on the same cell. This method can prove inaccurate for cells with very high series resistance due to the sloping of the curve near J_{sc}. Using the suns-V_{oc} method produces a curve much like the one-sun I-V curve except the effect of series resistance is removed since the measurement is only with an open circuit. This I-V curve is called the pseudo-I-V curve. Parameters such as pseudo-efficiency ($p\eta$) and pseudo-fill-factor (pFF) can be extracted from this curve in the same way as a typical I-V curve. These parameters are valuable in that the gauge the performance of a cell in which some aspects, such as the series resistance, are not optimized.

2.2.5 X-Ray Reflectometry

Grazing angle x-ray reflectometry can be used to measure the thickness of films that can not be measured via ellipsometry, visible/UV reflectometry or profilometry. Film roughness and density can also be determined using this technique. Figure 2.13 shows the result of such a measurement. Grazing angles less than the critical angle of total reflectance of incident x-rays are used to produce an interference pattern between reflections from the surface and underlying material interface.

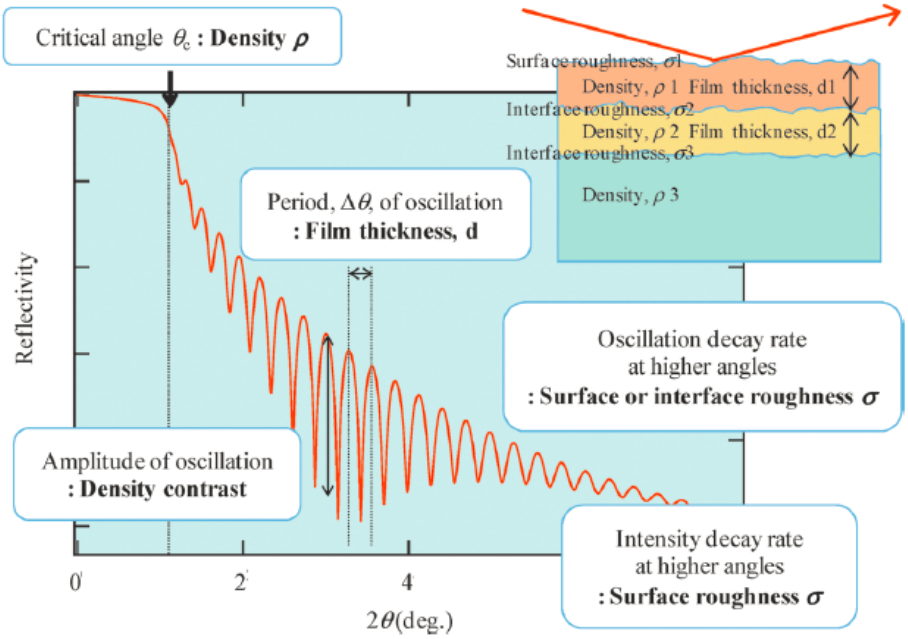


Figure 2.13: Typical XRR measurement and extractable parameters.[23]

Thickness can be approximated from Bragg's law, where the effect of refraction has been neglected.

$$d \approx \frac{\lambda}{2sin(\Delta\theta)} \tag{2.16}$$

where d is the film thickness, λ is the x-ray wavelength and $\Delta\theta$ is the difference in angle between the maxima as shown in Figure 2.13.

2.3 Review of Ni/Cu Front Metallization for Silicon Solar Cells

Ni/Cu/Sn front metallization schemes have been examined in the literature, where the Ni acts as the Cu diffusion barrier and Sn acts as a capping layer to prevent Cu oxidation. Several different processing methods have been explored and in these studies the Ni/Cu/Sn has shown efficiencies in the 16-21% range, often matching and sometimes outperforming their Ag counterparts. SunPower achieved a record 24% efficiency from Ni/Cu/Ag metallization plated over patterned Al.[6]

Despite these promising results, the long-term performance of Cu based metallization schemes remains a major concern. In the work of Bartsch et al. [9], the long-term stability of Ni/Cu/Sn front metallization was investigated. This was acheived by monitoring the degradation in pFF at 200 °C. This method allows for the replication of the thermal profile the cell would experience over hundreds of years in just a few days. The cells were fabricated by aerosol printing and firing a Ag seed layer through a SiN_x ARC followed by light-enhanced electroless plating of Ni and light-induced plating (LIP) of Cu. The results shown in Figure 2.14 confirms the need for a Cu diffusion barrier (other than the thin Ag seed), and illustrate that Ni is extremely effective. A 5% (relative) degradation of the devices with a Ni barrier and a thin seed represent the thermal equivalent of about 1000 years at 80 °C.

Screen printing is currently the industry standard front metal deposition method.

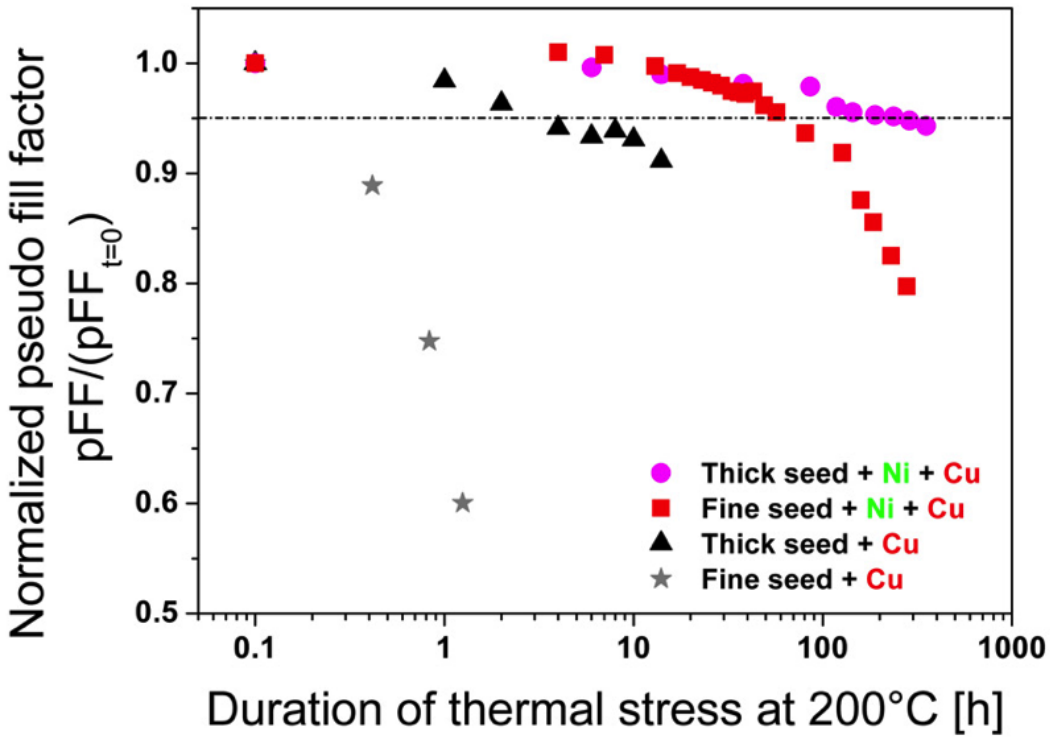


Figure 2.14: The degradation in pFF under 200 °C temperature stress.[9]

However, as the industry is moving to thinner substrates a non-contact deposition method is desirable. Additionally, the growth of interest in alternate metals, such as Ni/Cu, have furthered the interest in non-contact front metal deposition techniques such as plating of Ni and Cu which are well developed in the semiconductor industry. The ITRPV projection for increase in plating processes used in solar cell production is shown in Figure 1.3. However, if plating is to become the primary deposition method, a low cost process which allows patterning of the ARC is necessary. Direct chemical etching involves the direct application of an etchant in a defined pattern. An example of this is the printing of phosphoric acid paste followed by curing. Chemical etching can also be performed after a separate patterning process step (such as lithography or printing), but this method is not viable for high throughput, low cost production. Laser assisted methods, which involve a laser cutting through the ARC, and mechanical methods such as diamond blade sawing also have a potential role in future ARC patterning as the accomplish ARC etching in a single step.[6] Ni based fritted inks offer possibly the best option as they combine patterning, etching and Ni deposition into a single step. Methods such as inkjet printing where small nozzles are used to deposit ink droplets onto a substrate, are of great interest due to the simplicity of the process and compatibility with the trends of the PV industry. Once the ARC has been etched in some fashion, there are various methods of deposition which meet the needs of the PV industry very well. Unlike PVD methods like sputtering and evaporation, plating offers high deposition rates, simple processing, and therefore high throughput.

Electroless plating does not involve current flow and therefore electrodes and a

conducting surface is not needed to achieve deposition. This makes electroless plating well suited to act as the deposition method of the seed (Ni), to which a thicker layer of metal (more Ni then Cu or Cu) could then be electroplated at much higher deposition rate. Making use of the photovoltaic effect, light-assisted electroless plating has also been used to increase deposition rates in electroless plating. Results using this method of Ni seed deposition and subsequent Ag plating have resulted in efficiencies greater than 20% and FF higher than 80%.[24] Ni/Cu schemes achieved a greater than 20% efficiency by electroless plating of Ni and rapid thermal processing (RTP) to create NiSi which lowered the contact resistivity to $3.5 \times 10^{-7}\,\Omega\,\mathrm{cm}^2$, which is less than half that of the similarly process Ti/Pd/Ag cells.[25] Laser-assisted methods have made use of the photovoltaic effect as well. This method also increases the deposition rate due to heating at that location and the plating step can be combined with laser etching of the ARC, with some caution. This laser-assisted method can lead to excessive metal diffusion, and has not shown promising results for solar cells.

Electroplating takes place by means of metal ions migrating to a surface due to an applied electric field and reducing to form the metal layer. This does not require an additional reducing agent, unlike electroless plating. Since the deposition is due to the applied bias, non-uniform deposition can occur far from the external electrode contact due to resistance in the seed. LIP follows the same principle as electroplating but rather than the application of bias the photovoltaic effect is used to attract metal ions. This offers the benefit of uniform deposition since the front of the cell is not contacted. Deposition at the back of the cell can be controlled by contacting an additional electrode to the back of the cell. Electroplating and LIP are of value when

a seed is formed from printing, electroplating, or by other means because they quickly thicken the gridlines, reducing series resistance, while remaining separate from the formation of the contact to silicon.

Adhesion and durability are also major long-term concerns for the implementation of a Cu-based metallization scheme. While the adhesion between Ni and Cu is quite strong, the adhesion of the metal stack to Si can be problematic. Plating thick Cu lines induces a great amount of stress on the metal stack. This combined with mediocre adhesion of Ni to Si can cause flaking or peeling of the entire gridline. It has been shown that Ni silicidation can greatly improve the contact adhesion.[26] Removal of unreacted Ni after silicidation also improved adhesion.

2.4 Properties and Applications of NiSi

NiSi has been used extensively in industrial applications, especially in the IC industry as a contact to the source, drain, and gate in CMOS technology. There are a number of advantages NiSi provided over its predecessors, $CoSi_2$ and $TiSi_2$. As the industry moved past the 50 nm node, large increases in $CoSi_2$ line resistances were observed, which is essential the same issue that faced by $TiSi_2$ below the 350 nm node. Figure 2.15 shows this evolution.

This issue of high resistance is primarily due to the mechanism of phase formation.[28] $CoSi_2$ is nucleation controlled, producing a rough, non-uniform film while NiSi is diffusion controlled, resulting in a uniform, smooth film. The nature of the film formation is not only important in the resulting resistance, but in the CMOS industry was very important as silicon thicknesses on silicon on insulator (SOI) substrates grew thin.

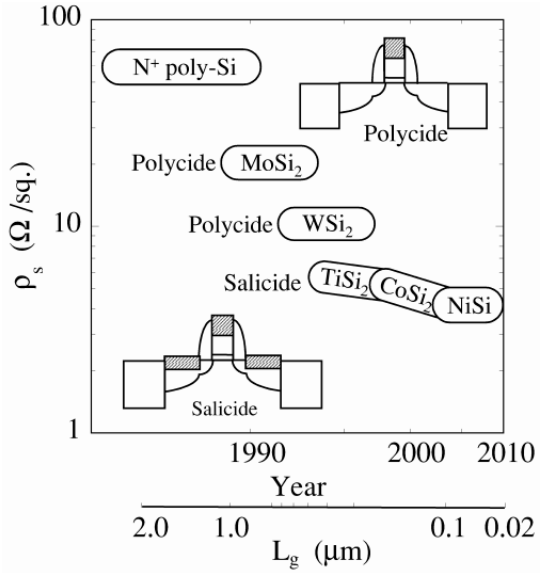


Figure 2.15: The evolution of CMOS silicide technology.[27]

The smooth nature of NiSi reduced the likelihood that a grain may penetrate through the silicon down to the insulator. In addition to this, the consumption of silicon is notably less in NiSi, due to both the decreased resistivity as well as the stoichiometry of the film and reduced density of Si. These same properties are important in assuring that the silicide does not contact the buried, tunneling oxide in passivated contacts in solar cells! Yet another benefit NiSi brings is a low thermal budget. The phase diagram of the Ni/Si system is shown in Figure 2.16. This is significantly more complicated than the Co/Si system allowing six phases of Ni/Si to be stable at room temperature and only three for Co/Si. Figure 2.17 shows the resistivity of Ni silicides and Co silicides at different annealing temperatures. The two curves of Figure 2.17 are shifted away from each other for clarity. Nickel monosilicide (NiSi) is the lowest resistivity phase of the Ni/Si system. Not only does the low resistivity, NiSi, phase form at lower temperatures, but there is a wider window of formation of this phase

allowing for process flexibility. Some of the important properties of NiSi and its other phases are summarized in Table 2.1.

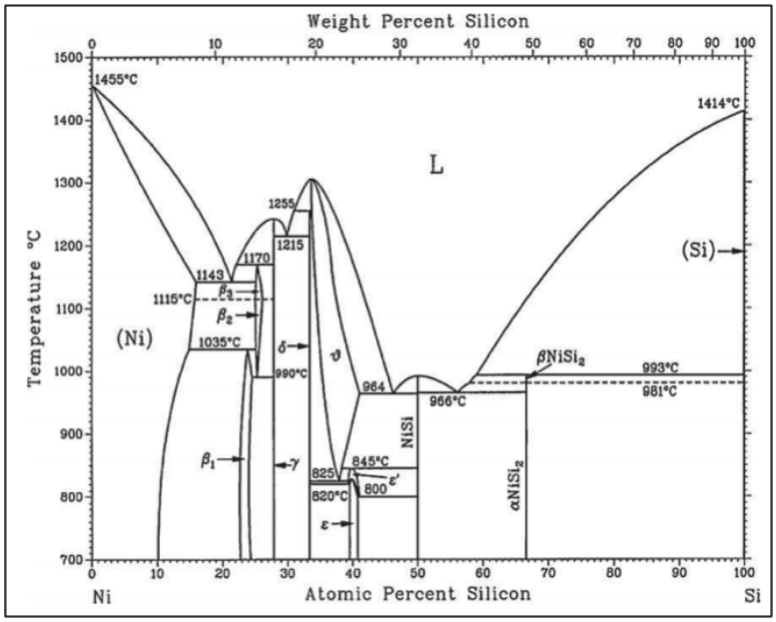


Figure 2.16: The phase diagram of the Ni/Si system.[29]

Phase	Resistivity ($\mu\Omega$ cm)	Structure	$t_{Silicide}/t_{Ni}$	$t_{Si\ Cons.}/t_{Ni}$
Ni	7-10	Cubic	1	0
Ni_3Si	80-90	Cubic	1.31	0.61
$Ni_{31}Si_{12}$	90-150	Hexagonal	1.40	0.71
Ni_2Si	24-30	Orthorhombic	1.47	0.91
Ni_3Si_2	60-70	Orthorhombic	1.75	1.22
NiSi	10.5-18	Orthorhombic	2.20	1.83
$NiSi_2$	34-50	Cubic	3.60	3.66
Si	Dopant Dependent	Cubic	-	-

Table 2.1: Properties of the room temperature-stable phases of the Ni/Si system.[28].

Nickel monosilicide can be formed by either a one- or two-step process. The one step process involves deposition of Ni and annealing at a temperature in the range of 350 °C to 650 °C. In the two-step process Ni is deposited and annealed in the 250 °C to 350 °C range for Ni_2Si formation. Unreacted Ni can then be etched followed by

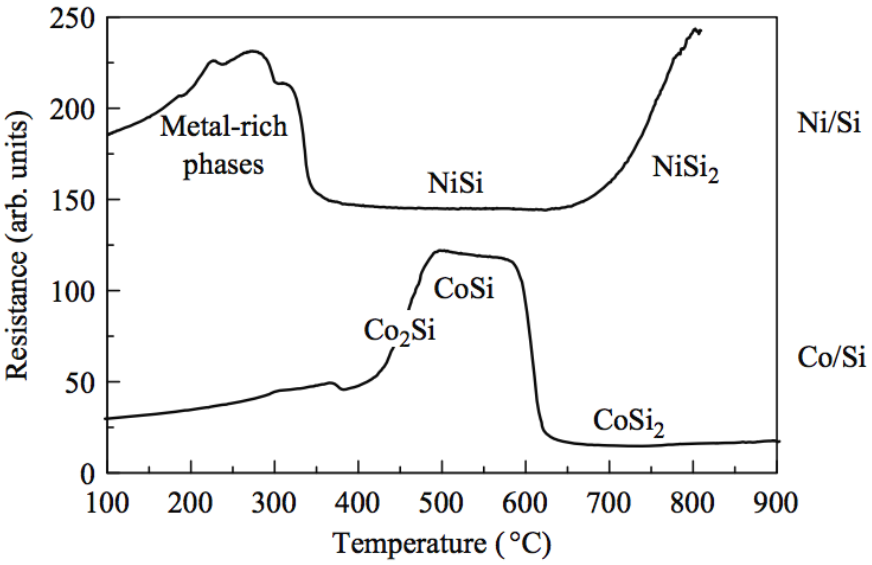


Figure 2.17: The resistivity of Ni silicides and Co silicides at various annealing temperatures. The two curves are shifted away from each other for clarity.[28]

a 450 °C anneal to produce NiSi.[30] This is generally understood to form a more uniform and higher quality silicide, and can typically be accomplished with a lower thermal budget. However, the complications added by this two-step process are not suitable for the high throughput demands of the PV industry, and the precision gained with this two step process is not necessary in most cases.

2.5 Advanced Devices

Due to the material advances made in silicon photovoltaics, one of the main limiting factors in their efficiency has become the surface recombination rate. The surface or interface of a any material(s) is inherently imperfect as it represents an abrupt change, but this is especially relevant for a highly crystalline material such as Czochralski grown (Cz) Si. Dangling bonds and crystal imperfections are a major source of recombination, as well as the mid-band states made available by diffusion of metal

atoms into the silicon during contact formation. One avenue to mitigate this is through the use of a passivated tunneling contact. The general structure of such a cell is shown in Figure 2.18.

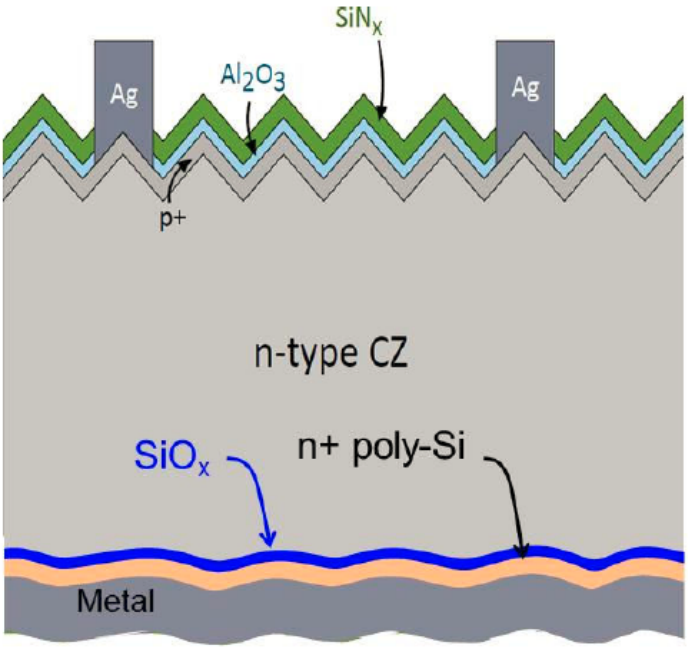


Figure 2.18: Cell structure with a rear passivated contact and passivated emitter.[31]

Passivation is achieved by reducing the concentration of recombination sites at the surface. This can be accomplished quite well by silicon dioxide (SiO_2) or alumina (Al_2O_3). Very thin films are of particular interest as they do not contribute a significant amount of stress, creating surface or bulk imperfections. On the front of the cell shown in Figure 2.18, alumina is used to passivate the area under the ARC. The rear of the cell in Figure 2.18, SiO_2 is being used as both a passivation layer and as a tunneling contact. This allows the large rear contact area, which would otherwise have a very high surface recombination rate, to be passivated while also maintaining

good, near-ohmic contact.

Tunneling oxide passivated contacts consist of a thin, insulating, tunneling, oxide layer with low interface trap density, followed by a "transport layer" in which a carrier can find an available state and thus transfer current. Passivated contacts reduce the loss mechanism by eliminating the defect density interface while still providing means to manage the transfer of current via quantum tunneling.[32]. Given an appropriate work function, the transport layer can be also be used to induce a junction in the base, resulting in field-effect passivation to supplement the chemical passivation of the tunneling layer. This allows for processing relating to BSF doping to be eliminated while maintaining the benefits.

Passivated tunneling contacts offer promise for applications in high efficiency silicon solar cells.[33][31] However, optimal metallization schemes for passivated contacts remain unclear. Currently, evaporated silver (Ag) metallization preserves the passivation quality of the contact, but presents both adhesion and cost issues. Moving to an alternate metallization scheme using electroplated copper is an attractive option. However, Cu diffusion in Si must be prevented with an appropriate barrier that also provides good contact resistivity to the poly-Si transport layer and maintains the passivation quality of the tunneling contact.

Chapter 3

Experimental Approach

A solar cell process was developed for RIT's Semiconductor and Microsystems Fabrication Laboratory (SMFL) which allowed for the comparison of different metallization schemes and the characterization of NiSi as both a contact and Cu diffusion barrier. Producing a very high efficiency cell was not the objective. It was however important to ensure the cells were of sufficient quality that degradation effects from the metal could be observed. Processes developed in this work were also tailored to investigate high efficiency passivated tunneling contact solar cells.

3.1 Solar Cell Design

The process flow for NiSi/Cu/TiN solar cells produced in this work has been summarized in Figure 3.1. Cross sectioned diagrams summarizing the major process steps are shown in Figure 3.2. Three lithography layers were used; one to define the mesas which isolate each cell or test structure, one to define the NiSi gridlines by etching "windows" in the ARC for self-aligned silicidation, and one to define the metal atop the NiSi, which was patterned by liftoff. The mask design is shown in Figure 3.3. The process was designed for 100 mm wafers. Each wafer has a total of 11 complete solar cells, each on their own isolated mesa. The dimensions of the mask defined cells

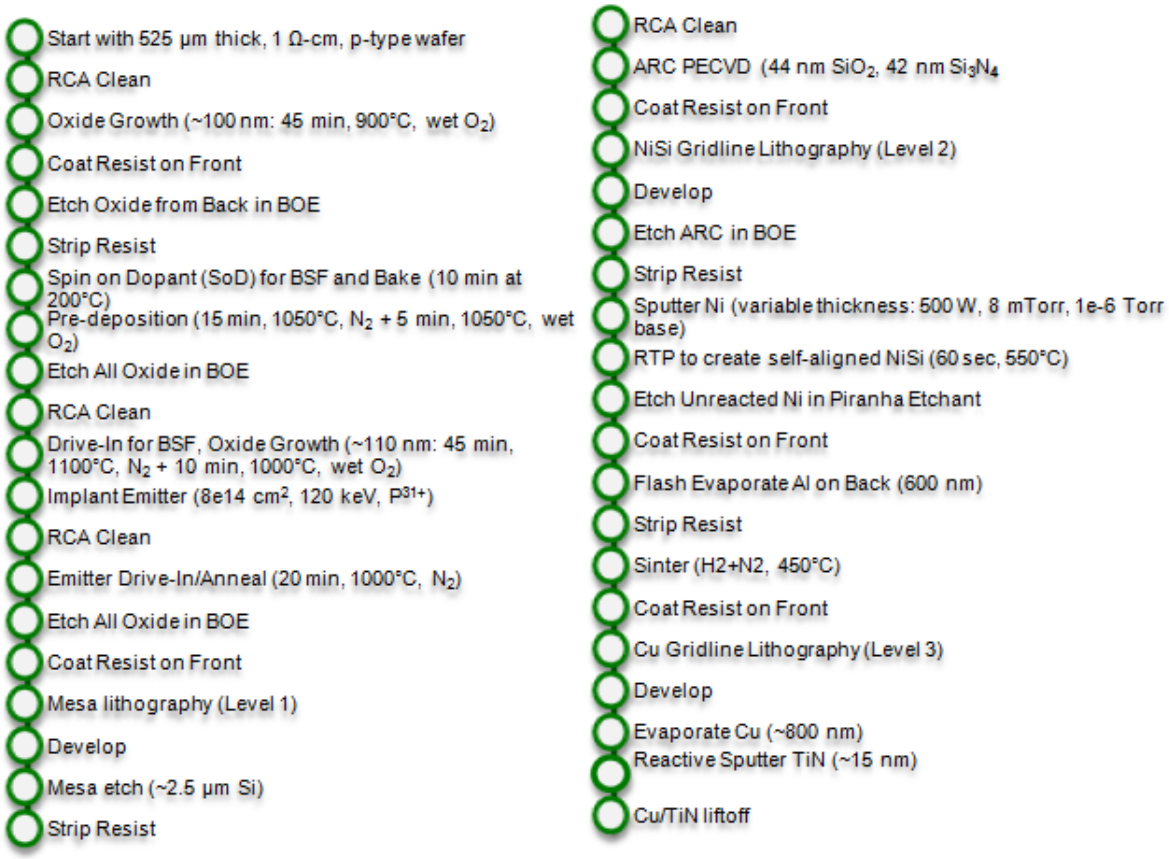


Figure 3.1: The entire process flow for producing mesa isolated solar cells with a BSF, two layer PECVD ARC, and NiSi/Cu/TiN contacts.

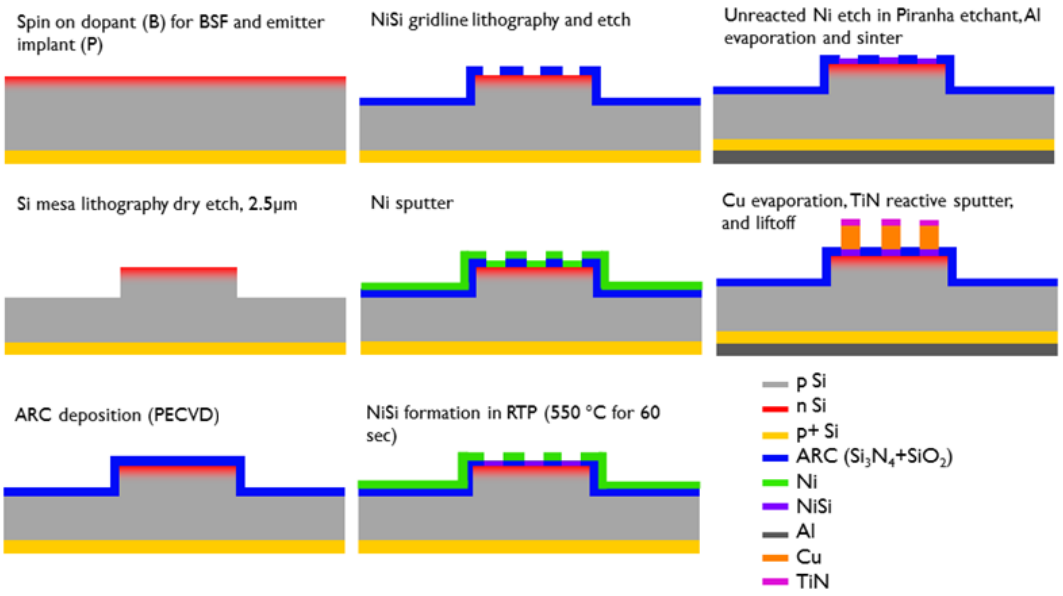


Figure 3.2: A diagram of the basic processing steps involved.

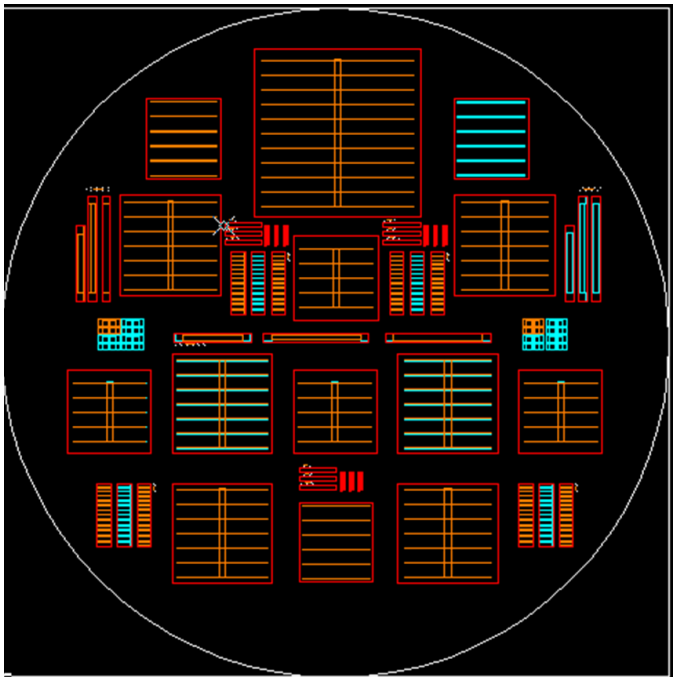


Figure 3.3: The mask design.

and gridlines are shown in Table 3.1. The mask patterns one 2.5 cm^2 cell, a total of four 1.5 cm^2 cells, two of each of the two variations on finger and busbar dimensions, and four 1.25 cm^2 cells. The mask defines 2100 µm spacing between each finger. To ensure the metal does not directly contact the silicon or the ARC, the NiSi gridlines are 20 µm wider on each side. The objective of this study was to evaluate NiSi as a Cu diffusion barrier, not the ARC.

There are a number of other structures defined by the mask. This includes the following:

- TLM structures for measurement of contact resistivity and sheet resistance
- Alignment marks to align the three mask levels
- Resolution test structures
- Alignment test structures
- Independent busbars
- Independent fingers

The TLM structures come in three varieties: NiSi only, metal only, and NiSi + metal. The dimensions of the TLM structures are summarized in Table 3.2.

3.2 Solar Cell Process

The substrates used in this experiment were 525 µm thick Czochralski grown silicon wafers with a 100 mm diameter and a resistivity range of 1-5 Ω cm, doped with boron. The process began with an RCA clean to remove organic and metallic contaminants

Mesa Dimensions (cm)	Mesa Area (cm^2)	Metal Dimensions (µm)	Number of Fingers	Shading (%)
2.5 × 2.5	6.25	Fingers: 22000 × 100 Busbars: 22100 × 850	11	6.88
1.5 × 1.5	2.25	Fingers: 13000 × 100 Busbars: 13300 × 700	7	8.18
1.5 × 1.5	2.25	Fingers: 12000 × 100 Busbars: 13300 × 1050	7	9.94
1.25 × 1.25	1.5625	Fingers: 10000 × 100 Busbars: 8900 × 875	5	8.18

Table 3.1: Dimensions of the solar cells and gridlines.

Pad Dimensions, $L \times Z$ (µm)	Mesa Width, W (µm)	Spacings, d (µm)	Number of Spacings, N
600 × 2000	2080	20-240 by 20	12
300 × 600	680	20-240 by 20	12
100 × 100	180	20-240 by 20	12
100 × 100	180	100-400 by 50	7
100 × 100	180	8-20 by 3	5
100 × 100	180	5-20 by 5	4

Table 3.2: Dimensions of the TLM structures.

before the first thermal step. A 100 nm field oxide was then grown in a steam ambient at 900 °C for 45 min. The front of the wafers were then spin coated with AZ 1518 photoresist and the oxide from the rear was wet etched in 5.2:1 buffered oxide etch (BOE). The resist was stripped using an NMP (1-Methyl-2-pyrrolidone) based solvent immersion stripper at 90 °C. Filmtronics B150 spin on dopant (SoD) was applied as the boron dopant source for the cell's back surface field (BSF), which provides field effect passivation at the rear contact. SoD provides a high dose alternative to what would be a lengthy implant step needed to produce a strong BSF with RIT's single tool ion implanter. The spin on dopant was then baked for 10 min at 200 °C. A

diffusion step including 15 min in N_2 and 5 min in steam at 1050 °C was used for pre-deposition. All oxide was then etched in BOE, an RCA clean was performed and the BSF dopant was driven-in with a 45 min diffusion at 1100 °C in N_2 and 10 min oxidation at 1000 °C in steam. This grows 110 nm of silicon dioxide, which was used as a screen for ion implantation of the emitter. The emitter was then implanted with a dose of $8 \times 10^{14}\,\mathrm{cm}^{-2}$ P^{31+} at 120 keV.

Following implantation, a pre-diffusion RCA clean was employed to remove contaminants introduced to the wafer surface during ion implantation. The emitter was then driven-in and electrically activated with a 20 min diffusion in N_2 at 1000 °C. The screen oxide was then wet etched in BOE.

Following this processing, resist was coated on the front of the wafer, exposed with a mercury broadband Suss MA55 aligner, and developed in CD-26. This is the first level lithography and will be used to pattern mesas atop which the cells will later be defined. The mesas electrically isolate each cell. The mesa etch etches 2.5 µm of silicon with 150 sccm SF_6, 40 sccm O_2 at 300 mTorr with 150 W RF power. This is below the emitter-base junction shown in Figure 3.4. The mesa was etched in a LAM 490 AutoEtch. The resist was then stripped and the wafers were cleaned.

The antireflection coating (ARC) was deposited with an AME P5000 via RF PECVD. SiO_2 was deposited at 390 °C and the Si_3N_4 was deposited at 400 °C. The ARC consists of 65 nm of SiO_2 atop 40 nm of Si_3N_4. The second level lithography was performed in the same manner as the first however the NiSi gridline mask was used. The pattern for the gridlines was etched in the ARC using a timed BOE. This step removes the ARC from the gridlines as well as providing a pattern of exposed silicon

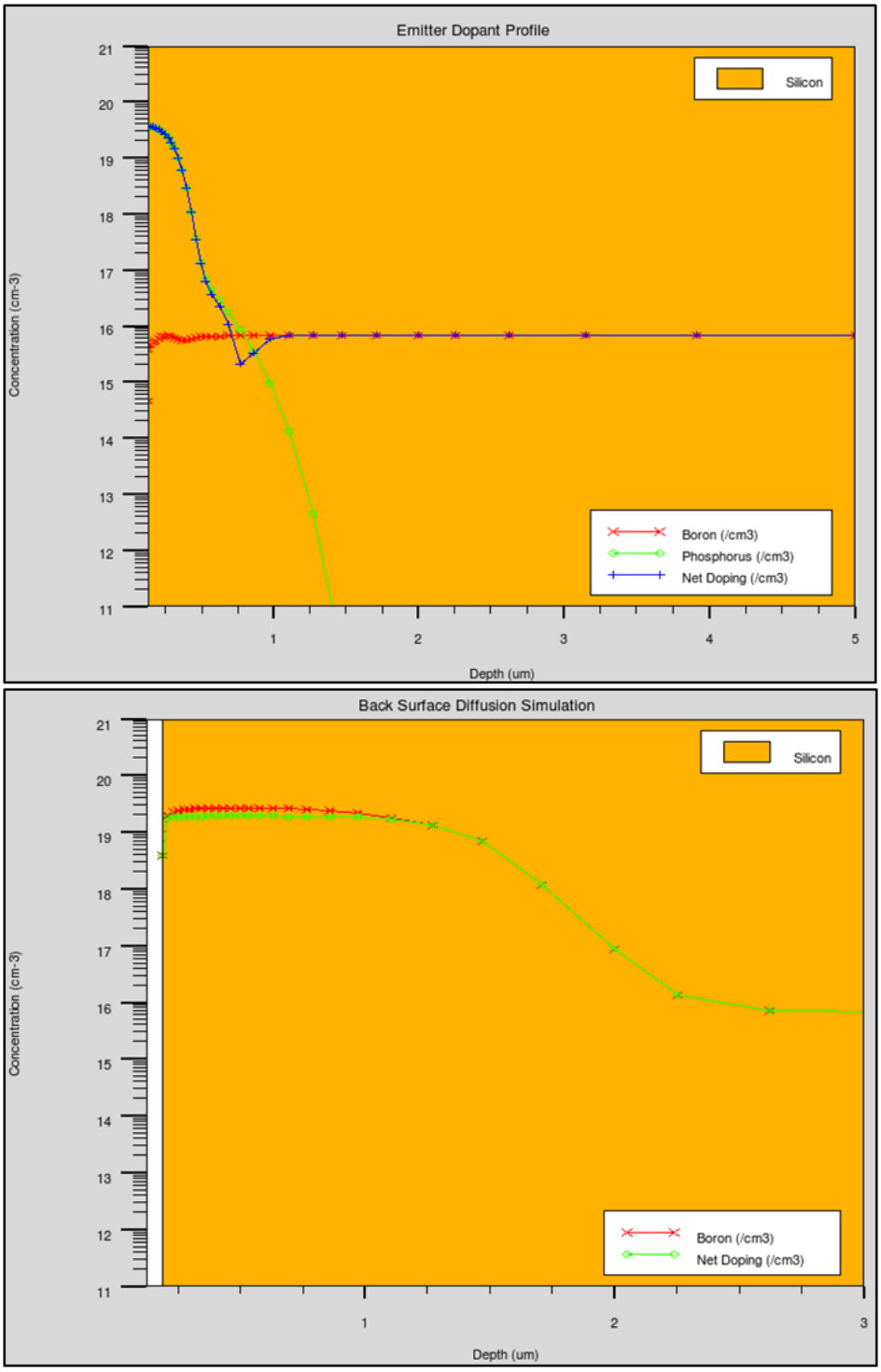


Figure 3.4: Diffusion profiles of the emitter and BSF implants.

where Ni silicidation can occur. The photoresist was then stripped.

Following a short dip in 50:1 BOE to remove native oxide, nickel was deposited in a Perkins Elmer 4400 RF sputter system using an 200 mm diameter Ni target and 500 W at 800 mTorr, on the 7 wafers designated for this processing. Ni was sputtered for 3, 4, and 5 min at approximately 9.5 nm/min. The Ni thickness was confirmed by X-ray reflectometry measurements. A 60 s rapid thermal anneal (RTA) at 550 °C in an inert environment (N_2) was used for the self-aligned silicidation (salicidation). NiSi phase formation was confirmed using X-ray diffraction (XRD) analysis. Unreacted Ni was then removed in a Piranha Etch (2:1 H_2SO_4:H_2O_2).

Photoresist was then coated on the front of the wafers. Using a CHA Flash Evaporator, 600 nm of aluminum was deposited on the rear of the wafer. The photoresist was stripped and the wafers were sintered in forming gas (5% H_2 in N_2) at 450 °C for 30 min. This process was originally intended to follow after front metallization however copper contamination of the tube could not be risked.

The third level lithography was performed to define the copper gridlines. This level uses LOR5A as an undercut layer below HPR504 photoresist. This process was found to be very sensitive. This was amplified by an oversight during process development. Initially copper was to be deposited with copper ink via an inkjet printer. Due to equipment limitations, it was not possible to print sufficiently thin gridlines. The copper liftoff process performed at RIT's SMFL was developed to compensate for this shortcoming. When the copper liftoff process was tested, it was tested on wafers which did not have NiSi gridlines. For the test, the ARC was deposited on a silicon wafer. The wafers were then coated with LOR5A and baked at 140 °C for 5 min. The

HPR504 was then coated, baked at 110 °C for 1 min. A small dose to clear DOE was performed to find an appropriate dose. The ARC was then etched in BOE. Copper was sputtered in a CVC 601 Sputtering System, depositing 360 nm of copper. This was then successfully lifted off in an ultrasonic bath of Remover PG.

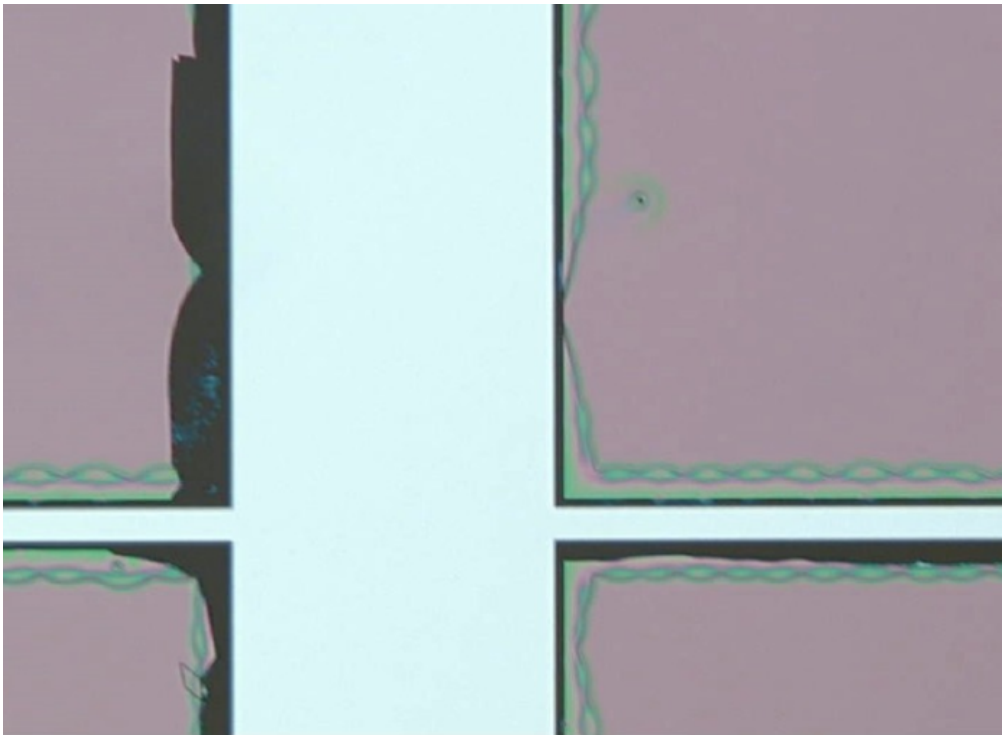


Figure 3.5: Poorly defined gridline pattern.

Due to this success, the full cells were processed under the same conditions. This yielded poorly defined lines as shown in Figure 3.5. In the original testing, the exposure implications of reflectance differences between the ARC and Si (Cu only cells) or NiSi were neglected. Additionally, it was found that the LOR5A soft bake was insufficient. A DOE on the softbake temperature and time was undertaken. It was found that 180 °C was needed for 5 min to achieve sufficient adhesion. Raising this bake temperature too dramatically adds significant time to the ultrasonic liftoff

process (>30 min). This was observed to cause copper lifting in some cases, as shown on the TLM structure of a test wafer in Figure 3.6. Due to this oversight, the full solar cells were reprocessed through this photo-loop multiple times, exposing the back metal and NiSi to the TMAH developer more than originally intended.

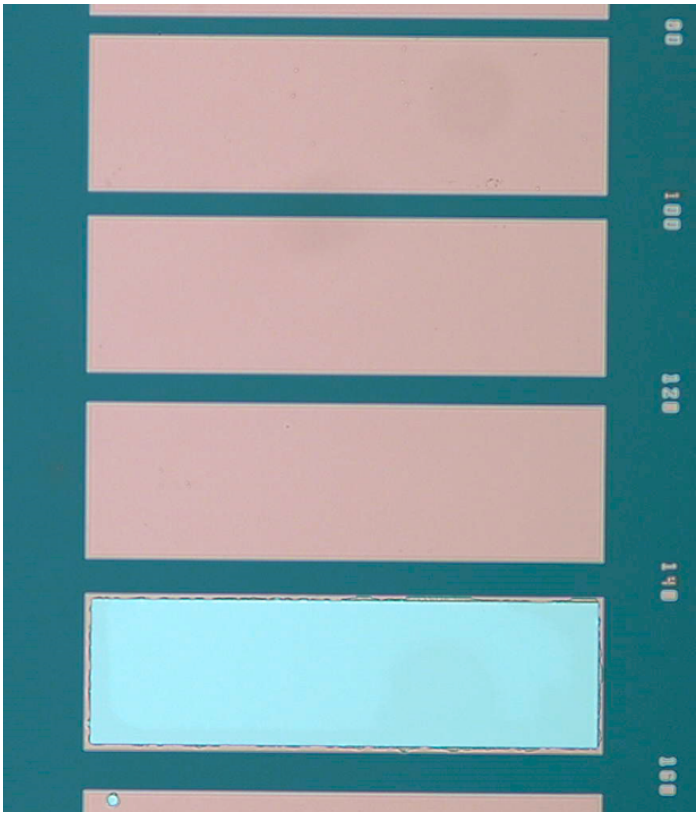


Figure 3.6: Copper lifting observed with extended time

The process continued as described for the test wafers except that 240 nm of copper were deposited to ease liftoff issues experienced in the metal lithography DOE. A TiN cap was reactively sputtered in situ in the CVC 601 Sputtering System as a cap to prevent oxidation of the Cu during thermal stress.

3.2.1 Alternate Metallization

Solar cells were fabricated with three metallization schemes, NiSi/Cu/TiN, Cu/TiN, and Ti/Pd/Ag. The wafers with Cu/TiN and Ti/Pd/Ag were processed the same as the cells with NiSi other than that Ni was not deposited, nor were they annealed for silicidation or exposed to the Piranha bath. Instead, they continued to the metal lithography.

30 nm of Ti, 30 nm of Pd and 500 nm Ag was deposited with a CHA electron beam evaporator. The Ti/Pd/Ag was lifted off in the same manner described for cells with Cu/TiN and NiSi/Cu/TiN.

3.2.2 Description of Samples

Eleven wafers were produced using the described processes. Seven wafers were metallized with NiSi/Cu/TiN, two wafers with Cu/TiN and two wafers with Ti/Pd/Ag. Of the seven wafers with NiSi, two had 38 nm of NiSi, two had 28.5 nm of NiSi and three had 19 nm of NiSi.

3.3 Passivated Tunneling Contacts for High Efficiency Cells

The NiSi/Cu metallization scheme was investigated on high lifetime passivated tunneling contacts fabricated and tested in collaboration with the National Renewable Energy Laboratory (NREL).[34]. These contacts were fabricated up to Ni deposition at NREL.

Symmetric passivated contact samples were prepared using 4 Ω cm, 180 µm thick, n-type Cz wafers. The wafer surfaces were etched with concentrated KOH to remove

saw damage and perform pyramidal texturing. Samples were cut and submitted to a piranha etch followed by an RCA cleaning procedure. Wafers were then treated with a high temperature, high cooling rate Tabula Rasa anneal to dissolve oxygen precipitates[35], re-cleaned via the RCA procedure before growing a 1.5 nm tunneling, thermal oxide at 700 °C in a quartz tube furnace. Next, the samples were loaded into an RF-PECVD reactor where 50 nm doped a-Si:P layers were deposited on both sides of the wafer.[31] Following another RCA clean, the samples were annealed in a dedicated quartz furnace at 850 °C, for 30 min to crystallize the a-Si:P layers into polycrystalline silicon (poly-Si) and to activate the P dopants. A TEM and band diagram of the tunnelling contact is shown in Figure 3.7. Hydrogen was diffused back into the poly-Si layer by adding a 50 nm layer of Al_2O_3, deposited by atomic layer deposition (ALD) over both sides of the samples, and then annealed at 450 °C for 30 min. This Al_2O_3 layer acts as a hydrogen reservoir to diffuse H to dangling bonds in the poly-Si and at the poly-Si/SiO_2/c-Si interfaces.[31] This treatment significantly improves the passivation of the contact layers, routinely giving implied open circuit voltages (iV_{oc}) over 730 mV by lifetime photoconductance decay (PCD) measurements.[22] For the samples in this study, iV_{oc} values near 700 mV were measured before the NiSi contact layers were added.

At this stage in the process, metal (Ag or Al) is typically added to the poly-Si layer after an HF etch to remove the Al_2O_3 layer. For this study, however, it was found that forming NiSi to the poly-Si directly significantly reduced the passivation of the contact. This reduction was most likely due to thick NiSi layers that consumed the poly-Si down to the SiO_2 layer, or Ni diffused through the poly-Si grain boundaries

and destroyed the SiO_2 interface. To prevent this degradation to the passivation quality of the contact, 50 nm of a-Si:P on top of the poly-Si layer was added before forming the NiSi contact. Care was taken to form less than 20 nm of NiSi to maintain an amorphous film over the poly-Si layer that was void of grain boundaries to prevent Ni diffusion. The results were a significant improvement in the passivation quality of the contacts.

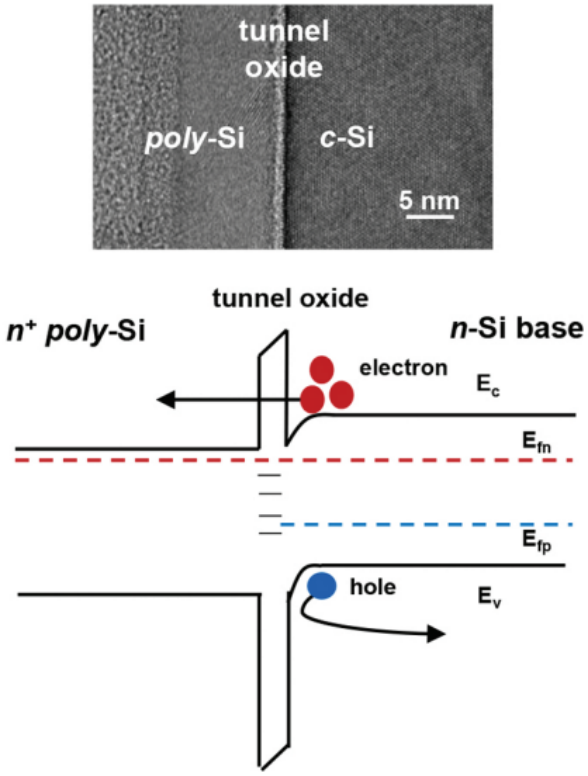


Figure 3.7: Transmission electron micrograph of the tunneling contact and the associated band diagram.[17]

Four different NiSi thicknesses were formed nominally 10, 12, 15 and 19 nm. NiSi thicknesses less than 10 nm yielded very high resistivities. This is likely due to silicon rich phase formation since the RTA process was develeped for thicker NiSi. Based

on the known consumption of silicon shown in Table 2.1, these thickness of NiSi leave 34-42 nm of the a-Si:P cap. It was assumed that the consumption of a-Si is approximately the same as c-Si shown in Table 2.1. Nickel was deposited in a Perkins Elmer 4400 RF sputter system using an 8" diameter Ni target. The Ni thickness was confirmed by X-ray reflectometry measurements. A 60 s RTA at 550 °C in an inert atmosphere (N_2) was used for silicidation. Unreacted Ni was then removed in a Piranha Etch (2:1 H_2SO_4:H_2O_2).

3.4 Measurement Techniques

3.4.1 Transmission Length Method (TLM)

TLM measurements were made using a manual probe station since each contact spacing is different. A 4-wire approach was used to reduce error in the resistance measurement, producing and I-V curve across each spacing to determine resistance. An HP4145 parameter analyzer was used to sweep voltages between -1 V and 1 V, which maintained current in the mA range.

3.4.2 TLM Design and Error Analysis

In the course of this study, it was observed that contact resistance measurements in the PV field lack standardization. Due to this, inaccuracies and misconceptions can be introduced. To minimize this, the optimal TLM structure was sought out following the error analysis outlined by Ueng et al.[36]

Given a sheet resistance (of the emitter in this case) and a contact resistance, there is an optimally dimensioned TLM structure. This characteristic is demonstrated in Figure 3.9 and 3.8 for a contact resistance of 1 $\mu\Omega\,cm^2$ using a TLM structure with

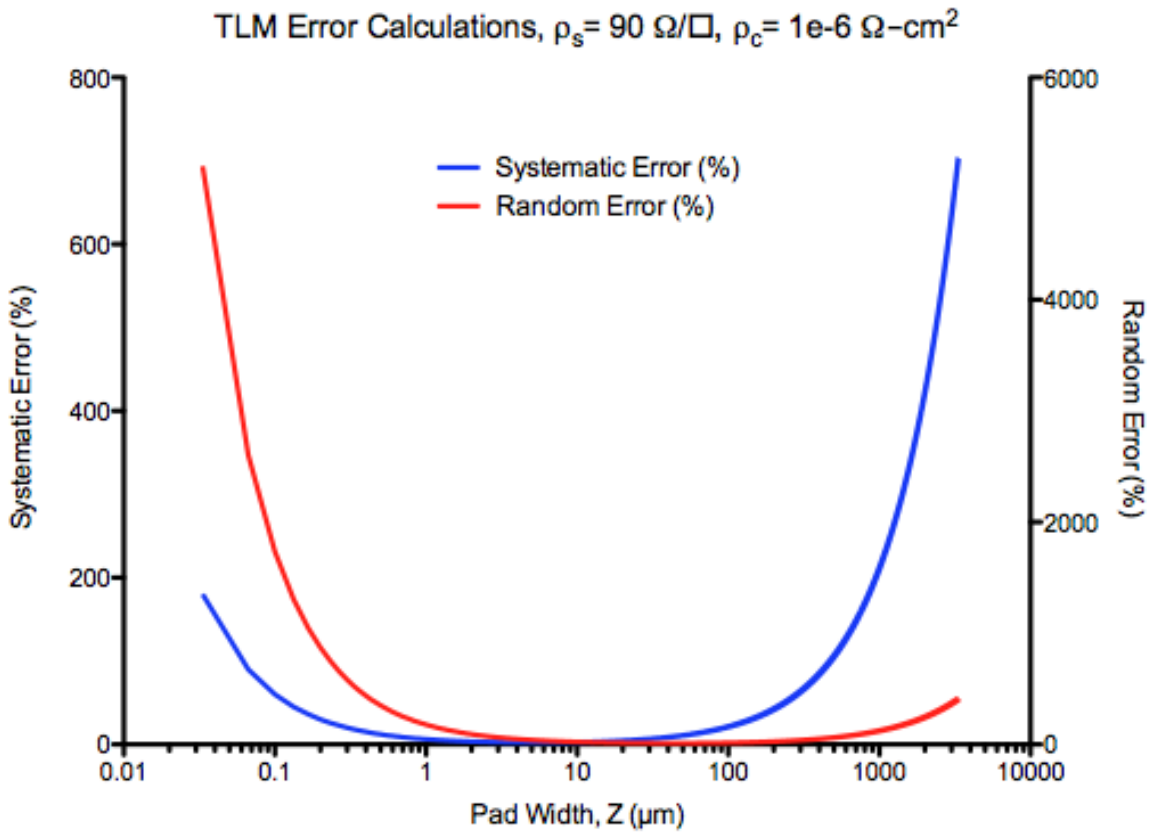


Figure 3.8: Random and systematic TLM error calculation as a function of pad width.

12 spacings, the largest of which is 240 µm. This calculation also assumes random and systematic error of 0.1 µm in the pad spacing, 0.2 µm in pad width and 0.2 Ω in the measured resistance between each set of pads. Figure 3.8 assumes the sheet resistance under the contact is 90 Ω (the targeted emitter sheet resistance of the devices produced in this work) while Figure 3.9 shows the calculated error over a range of sheet resistances.

Due to test apparatus and processing limitations, a pad width less than 100 µm was not fabricated. This issue is characteristic of a limitation in measurement accuracy in the PV industry as 10 µm lines are not easily produced via economically viable solar cell patterning techniques.

3.4.3 I-V Characteristic and Solar Simulator

The I-V characteristic of the solar cells were measured under a simulated AM1.5 spectrum using a 92250A-1000 Newport/Oriel Solar Simulator and Keithley 2440 SMU.

3.5 Device Degradation

The diffusion of Cu into the solar cell is the primary concern of Cu metallization schemes. It is therefore critical that any gauge of the Cu diffusion accurately reflect the device performance. For this reason, testing methods demonstrating degradation (or lack thereof) of actual solar cell operational parameters were used. This was accomplished by comparing quantum efficiency values before and after a Cu diffusing temperature stress as well as measuring pseudo-Fill-Factor (pFF) throughout the stress, as described by Bartsch et al.[9] The temperature stress endured was 200 °C

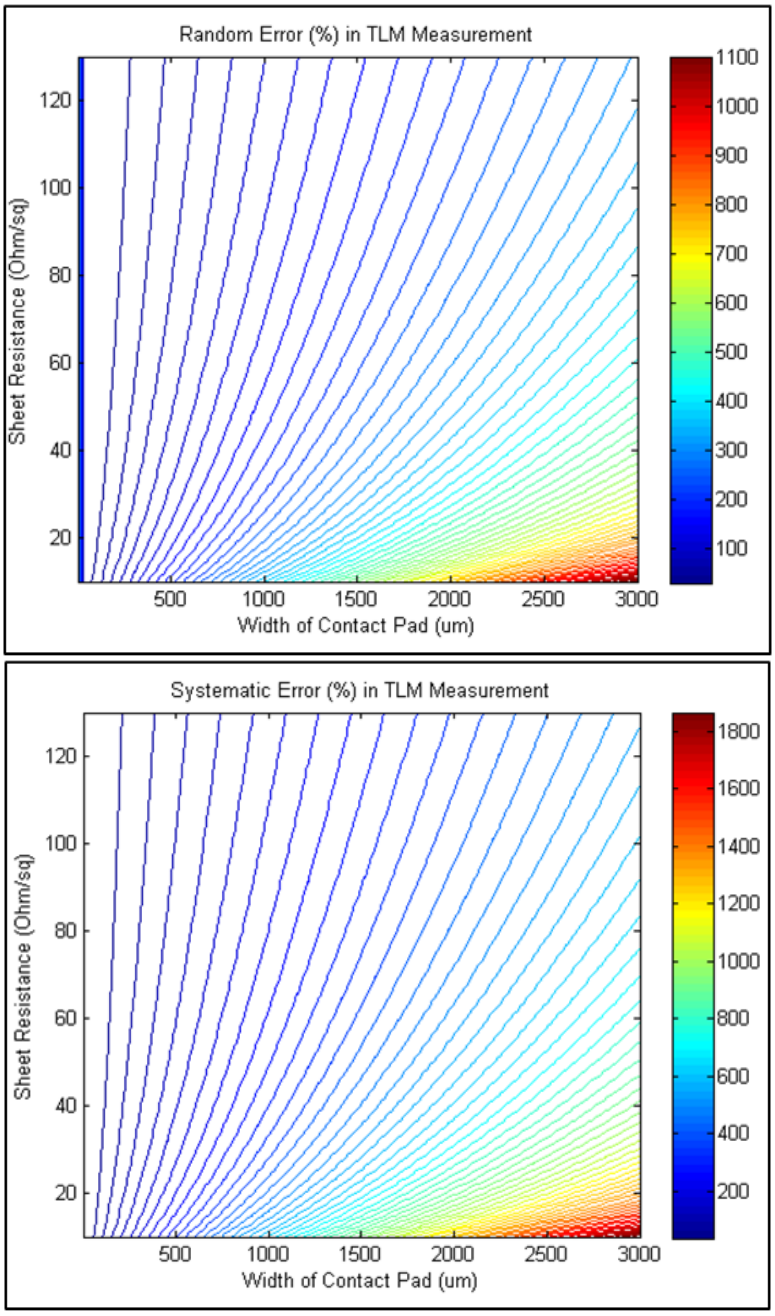


Figure 3.9: Random and systematic TLM error calculation as a function of pad width and emitter sheet resistance.

in air for 165 h using a hot plate.

Suns-V_{oc}

Suns-V_{oc} was measured using a Sinton suns-V_{oc} setup located at the SUNY CNSE Solar Rochester facility. All 11 solar cells were measured on 1 wafer of each treatment (3 metallization schemes, and 3 NiSi thicknesses). This was done successively over the course of the temperature stress.

Quantum Efficiency

Quantum efficiency was measured using a Newport/Oriel QEPVSI system consisting of a 300 W xenon arc lamp, Oriel Cornerstone monochromator with a chopped output, digital Merlin lock-in amplifier and NIST traceable silicon reference detector. Limitations on the adjustment of output beam size limited the cells which could be measured since the entire beam must incident on the cell area for accurate measurement.

Chapter 4

Results and Discussion

4.1 Material Characterization

4.1.1 X-Ray Reflectometry

Since Ni is opaque and this process calls for thicknesses too thin to reliably measure with a profilometer, X-Ray Reflectometry was used to characterize the film thickness and process deposition rate. Sample XRR data showing Ni thickness on Si is shown in Figure 4.1. A sealed tube x-ray source of Cu-Kα radiation ($\lambda = 1.54\,\text{Å}$) with a Huber 4 full circle diffractometer and was used for this measurement. Film thicknesses were determined based on the average $\Delta\theta$ and Equation 2.16.

Table 4.1 summarizes the measured resistivity of NiSi. These were determined by measuring the sheet resistance of NiSi on full wafer control samples with an automated 4-point probe. Resistivity was then calculated based on film thickness determined via XRR. Excluding one high and one low outlier, the measured resistivities match the literature value very well.

4.2 Contact Resistivity and TLM Measurement

4.2.1 TLM Measurement Results

TLM measurements were performed for NiSi contacts prior to Cu/TiN metallization and compared to a Ti/Pd/Ag contact. This illustrated that NiSi alone forms a

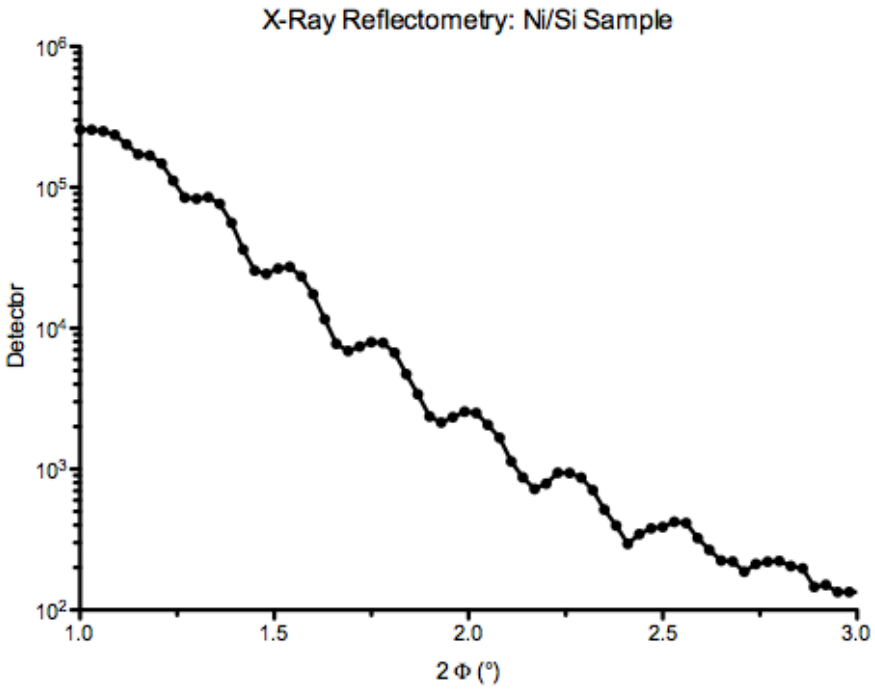


Figure 4.1: Sample XRR data from a Ni/Si sample.

Deposition Time(s)	**Thickness (nm)**	**Resistivity(μΩ cm)**
60	12	54.0
60	10	17.1
80	13	14.7
100	16	11.6
120	19	13.5
120	19	14.5
180	21	10.1
180	21	7.30
360	65	14.5
Average	-	**13.7**
Literature Value NiSi[28]	-	**10.5-18**

Table 4.1: Thickness and resistivity of NiSi control samples as measured by XRR, TEM and 4-point probe.

superior contact. As discussed in previous sections, the metal resistivity must be accounted for in the case of a silicide contact. Figure 4.2 shows the result of the TLM calculation both with and without the metal resistivity considered. Metal resistivity was measured via four point probe on a control wafer. Note that the change in the result is more drastic for NiSi, since its resistivity is much greater than that of Ti/Pd/Ag.

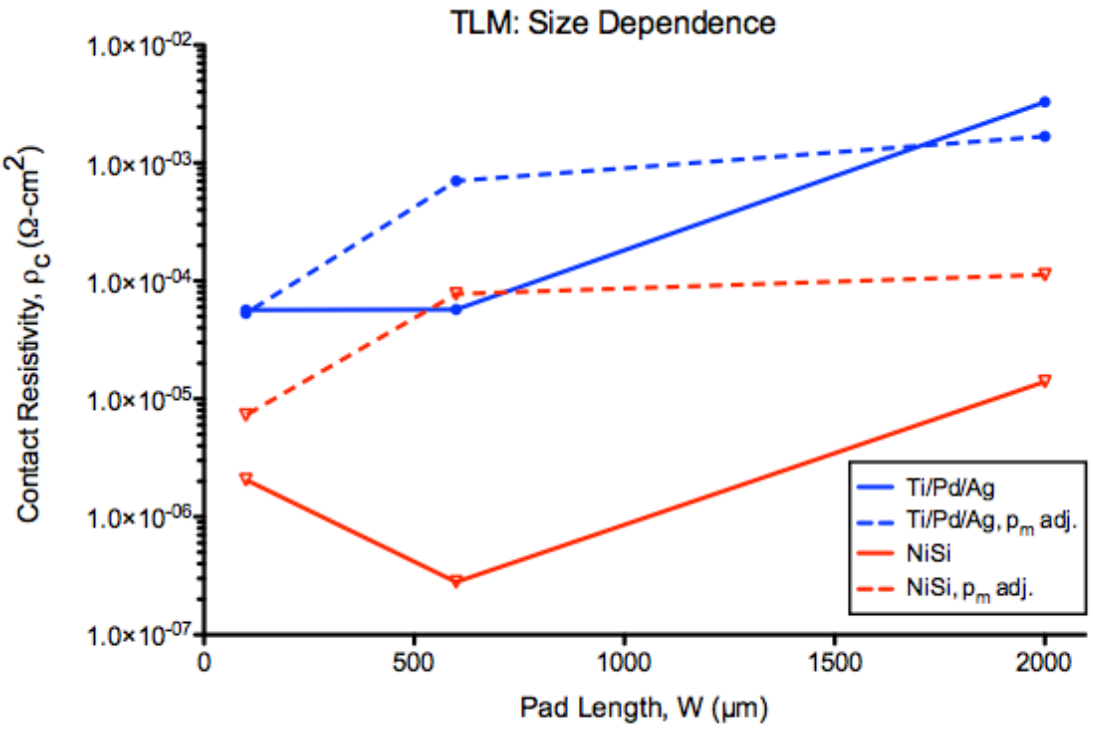


Figure 4.2: Contact resistances of Ti/Pd/Ag-Emitter and NiSi-Emitter contacts via TLM structures of various dimensions.

Figure 4.3 illustrates that the $2\,\mathrm{m\Omega\,cm^2}$ goal was achieved in the final devices despite the TiN/Cu system remaining non-optimized. This corresponds to less than 5% efficiency loss due to the resistance of the contact. The trend with thickness is likely due to purer nickel monosilicide phase formation for thicker silicides. This

implies that the RTA process is not optimal for all thicknesses of source Ni. It is likely the RTA time is too long for thinner Ni, forming Si rich phases.

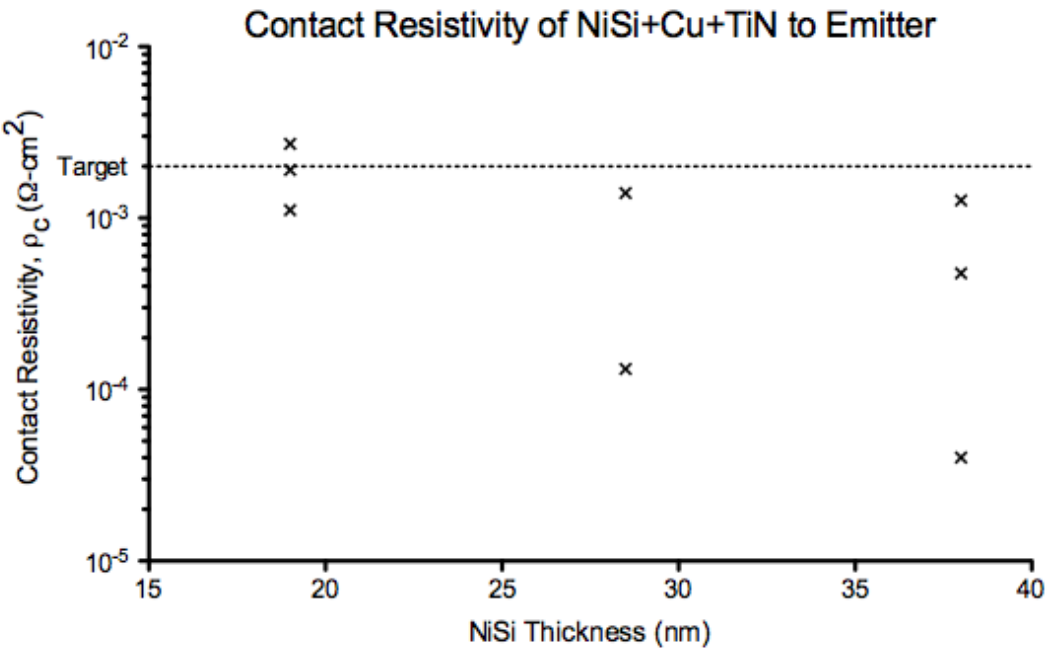


Figure 4.3: The measured contact resistance of the final devices with NiSi/Cu/TiN as a function of NiSi thickness.

In future work the silicidation process can be optimized by comparing the sheet resistance of samples with equal Ni thickness while varying the RTA time and temperature.

4.3 Solar Cell Performance

4.3.1 I-V Characteristic

The one-sun I-V and suns-V_{oc} characteristics of the most efficient solar cell produced in this work are shown in Figure 4.4. Performance parameters derived from these measurements are shown in Table 4.2. The cell performance was degraded significantly

by high series resistance and low minority carrier lifetime.

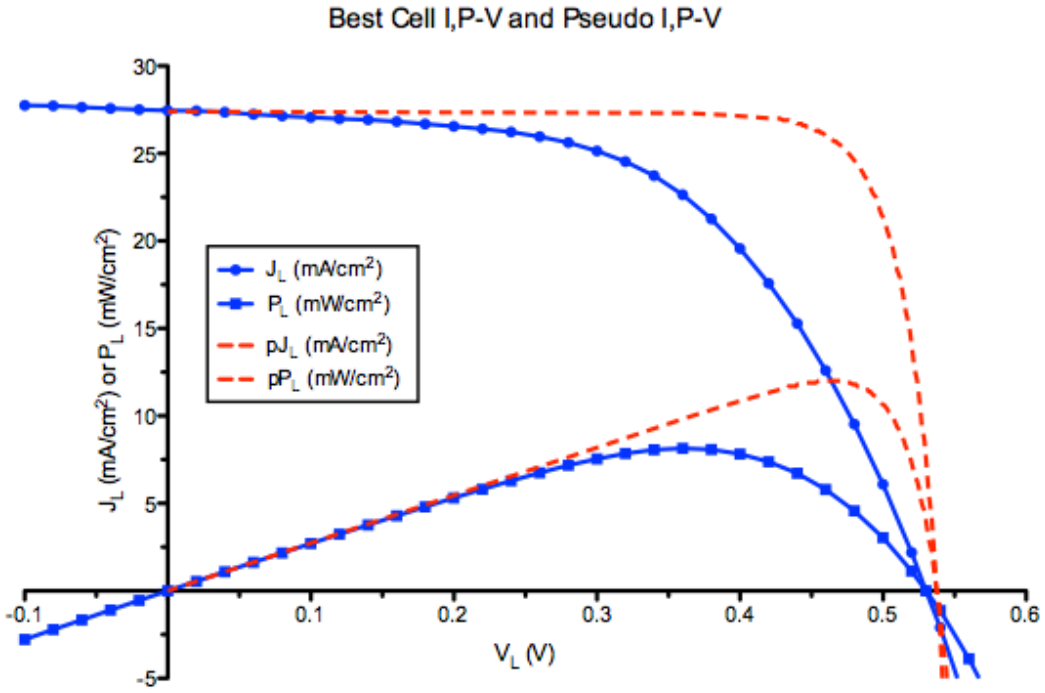


Figure 4.4: Suns-V_{oc} and one-sun I-V characteristic of the most efficient solar cell produced using the process described in this work.

4.3.2 Temperature Stress and Degradation

The temperature stress revealed that the TiN oxidation barrier was ineffective. The copper visibly oxidized after extended periods on the hot plate. Further process development is necessary to improve this failure mechanism. The difference is shown in Figure 4.5. The wafer on the left had Ni/Cu/TiN metallization and had not undergone any temperature stress. The wafer on the right had the same treatment (same metal stack and same NiSi thickness), except it was used for the temperature stress and the copper oxidized. Note the difference in color. The wafer above the others had only Cu/TiN and had undergone the temperature stress as well.

Figure 4.5: Visual comparison of wafers before and after temperature stress.

Measured Parameter	J-V 1 Sun	Suns-V_{oc} Scaled to J_{SC}
η (%)	8.15	-
$p\eta$ (%)	11.8	12.0
FF (%)	55.97	-
pFF(%)	81.2	81.2
V_{oc} (V)	530	538
J_{sc} ($\mathrm{mA\,cm^{-2}}$)	27.5	27.5
$R - V_{oc}$ ($\Omega\,\mathrm{cm^2}$)	4.6	-
$R - J_{sc}$ ($\Omega\,\mathrm{cm^2}$)	406	-
V_{mpp} (V)	362	464
J_{mpp} ($\mathrm{mA\,cm^{-2}}$)	22.5	25.8
n_1	2.50	0.94
J_{01} ($\mathrm{mA\,cm^{-2}}$)	7.08×10^{-3}	2.23×10^{-11}
J_{02} ($\mathrm{mA\,cm^{-2}}$)	-	1.00×10^{-11}
R_s ($\Omega\,\mathrm{cm^2}$)	2.06	0.89
R_{sh} ($\Omega\,\mathrm{cm^2}$)	-	3.50×10^{3}

Table 4.2: Measured electrical performance parameters of the best solar cell using a one-sun solar simulator and and Sinton suns-V_{oc} setup.

The result of the pFF test is shown in Figure 4.6. Each data point is the average of the 11 solar cells on each 4" wafer. All cells had initial pseudo fill factors in the range of 77-79%. From this it must be concluded that this test is insufficient in displaying degradation due to Cu diffusion for these devices. The Cu/TiN control cells did not degrade in any statistically relevant way. This is in conflict with the pFF results described by Bartsch et al.[9] as well as with the greater scientific community. The observed and measured series resistance issues due to Cu oxidation and rear aluminum etch damage could not have caused these issues since the suns-V_{oc} gauge of pFF measures only V_{oc} of the actual cell. This is superior to J_{sc}-V_{oc} systems in that J_{sc}-V_{oc} systems can be vulnerable to inaccuracy with very high series resistances where the I-V curve is sloped at J_{sc}. Suns-V_{oc} systems use a second, reference solar cell to gauge the level of irradiance. The suns-V_{oc} curve can be scaled to the known

J_{sc}. The insensitivity of this measurement was likely caused by globally low minority carrier lifetimes.

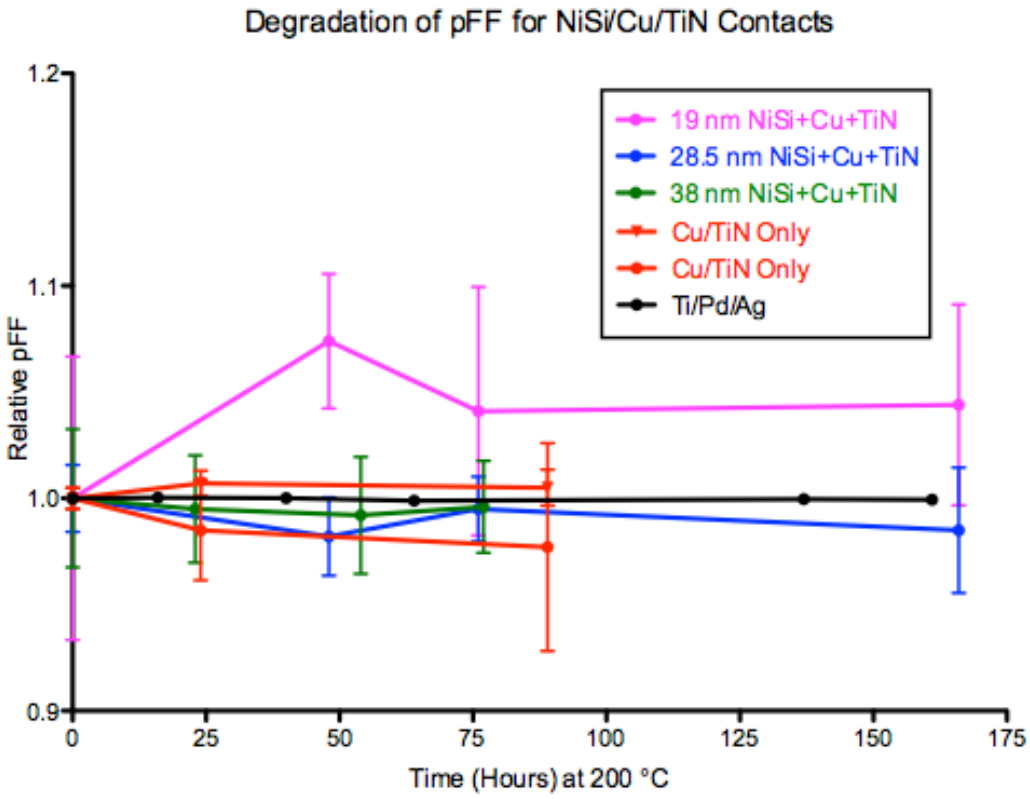


Figure 4.6: The pFF measurement for NiSi/Cu/TiN, Cu/TiN, and Ti/Pd/Ag metallized solar cells.

Despite the lack of a conclusive pFF measurement, the change in quantum efficiency before and after the temperature stress showed a clear trend. Figure 4.7 shows the absolute difference between the EQE before and after the temperature stress at the same location on each device. The Cu/TiN control cells degraded up to nearly 15% EQE at some wavelengths, while the NiSi/Cu/TiN cells did not degrade in any significant way. It is reasonable to infer that a cell with an initially higher minority carrier lifetime would experience a greatly exaggerated, but similar effect. This is

because in that regime a change in Cu concentration within the bulk would account for a larger fraction of trap sites. It is also strongly possible that a statistically discernable degradation in pFF would be observed had the initial bulk minority carrier lifetime been longer.

Figure 4.8 shows the two best QE curves for both a NiSi/Cu/TiN cell and a Ti/Pd/Ag cell. This illustrates that NiSi/Cu/TiN is capable of outperforming Ti/Pd/Ag in an absolute sense.

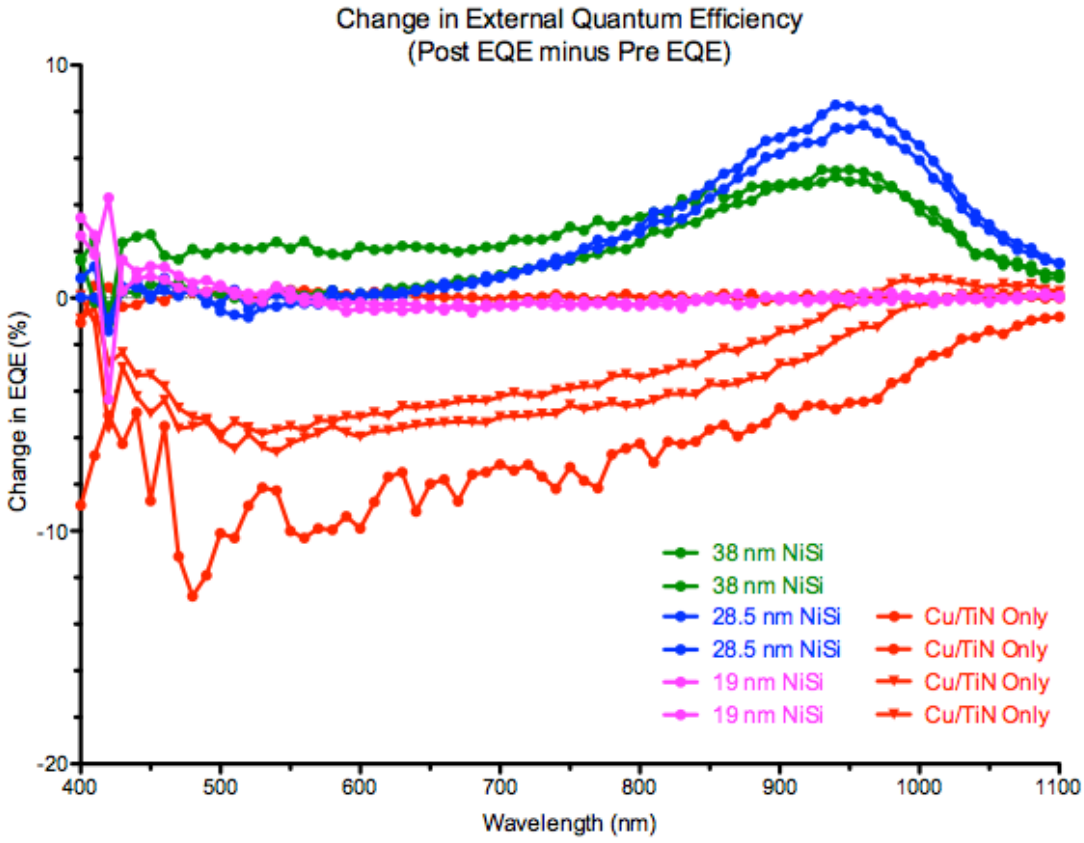


Figure 4.7: The change in EQE before and after thermal stress.

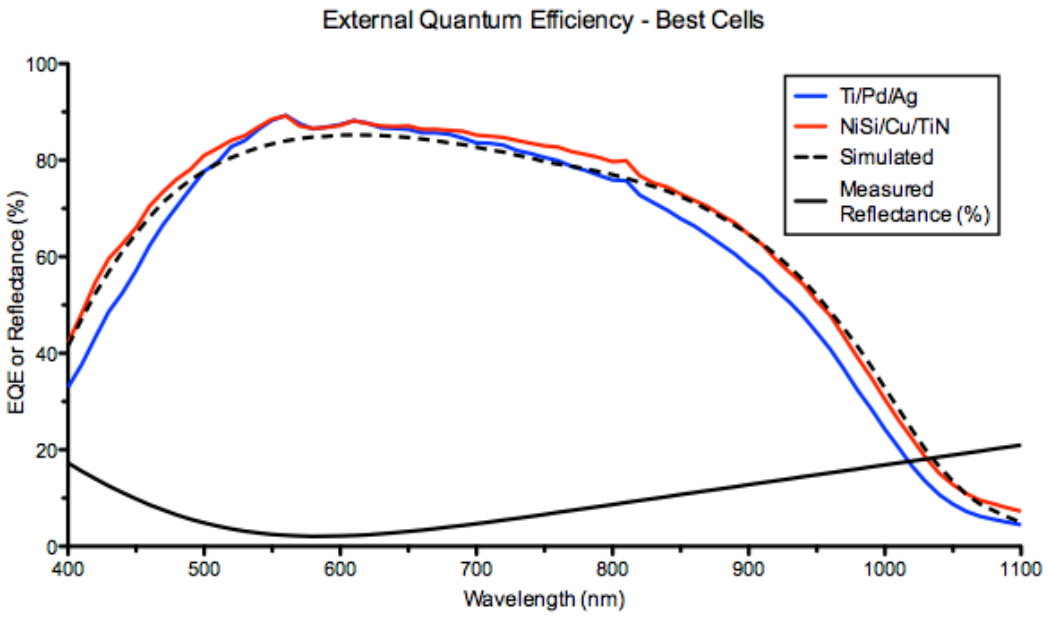


Figure 4.8: The best cell EQE for both the NiSi/Cu/TiN and Ti/Pd/Ag metallization schemes.

4.4 Process Discussion

Since the objective of this work was not necessarily to produce the most efficient cell possible, many factors involved with the process and design were not optimized.

4.4.1 Device Simulation

In future work, process parameters such as the emitter and BSF dopant profiles can optimized using PC1D to improve performance. The emitter and BSF dopant profile was simulated with Silvaco's 2D process simulator, Athena. The implant or predeposition diffusion was simulated respectively as well as all subsequent diffusions. The final simulated dopant profiles are shown in Figure 3.4. Since, PC1D cannot accept diffusion profiles as an input, the profiles were approximated as Gaussian using the peak doping and junction depth shown in Figure 3.4.

The targeted sheet resistance of the emitter for example was 90 Ω. In reality, it was measured closer to 110 Ω. This is a source of series resistance.

4.4.2 Reflectance

The second level lithography defined where the ARC was etched from the gridlines. Following this, the photoresist was stripped in an immersion bath. The wafers were then dipped in 50:1 BOE to remove a native oxide from the gridlines and Ni was deposited. Since the resist was already stripped, this dip etches the ARC globally. This etch therefore sets the final reflectance of the ARC. This BOE dip was done after the resist strip to minimize time and processing between the BOE dip and Ni deposition.

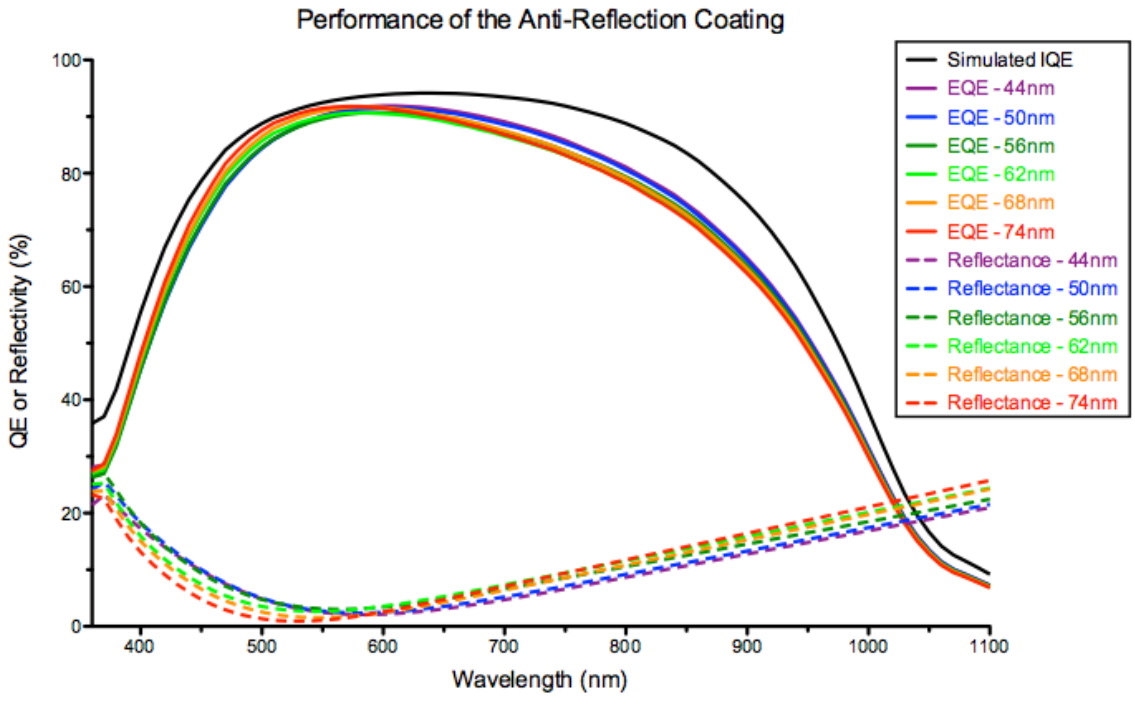


Figure 4.9: The measured reflectance of the ARC for successive pre-metal BOE process times and associated EQE based on simulated IQE.

The ARC was deposited on a silicon test wafer. The top layer SiO_2 was then step etched in six 6 s intervals from 74 nm to 44 nm. The reflectance of the ARC was measured with a Cary 500 integrating sphere spectrophotometer in RIT's Color Science Laboratory. This measurement was used to determine the most appropriate etch time. The simulated IQE is shown in Figure 4.9. Each reflectance measurement was used to calculate an EQE. As discussed in previous chapters, QE can appear ambiguous. The ultimate metric is the power efficiency under one-sun. PC1D was used to simulate the efficiency of the cell using the measured reflectance data from each segment of the step etched wafer. The resultant efficiencies are shown in Table 4.3. The longest etch, thinnest oxide was the most efficient cell in these simulations. This shows that the longer wavelengths, above 600 nm, where the 44 nm film is least reflective, are more important than shorter wavelengths, with respect to these reflectance curves.

Thickness (nm)	**Simulated AM1.5 Efficiency (%)**
74	13.5
68	13.5
62	13.4
56	13.5
50	13.6
44	13.7

Table 4.3: Simulated power conversion efficiency of the solar cell using measured integrating sphere reflectance as an input.

Ideally, the efficiency would have peaked and began to drop within the range of measured etches. Note that as thickness decreases, the reflectance curve shifts to the right. Continuing in this direction will result in an efficiency loss at a point

because the gained long wavelength collection will be overcome by the loss of short wavelengths.

Unfortunately, there was not sufficient time to repeat the measurement in RIT's Color Science Laboratory. Rather than making a blind process decision to etch more than what was measured, the device wafers were etched to the 44 nm target oxide thickness.

In future work, another step etch could be performed to find a true minimum reflectance. Additionally, the ARC reflectivity should be measured after all processes (especially following the Ni etch) to determine the optical effect of this processing.

4.4.3 Front Surface Passivation and the ARC

Via PC1D QE simulation and matching to measured QE, the front surface recombination velocity was found to be 3 cm. This could likely be reduced by using silicon dioxide as the bottom layer of the ARC as it yields superior passivation as compared to silicon nitride. A two layer ARC could still be used, however the effect of the Ni etch and following processing on the top ARC layer must be determined.

4.4.4 Lifetime Analysis of Fab Processes

The results of pFF and QE measurements, followed by simulation, indicate that the minority carrier lifetime is very poor. Simulation results indicate a minority carrier lifetime of approximately 2.8 µs. In future work, analysis of minority carrier lifetime should be gauged after each individual process to determine the primary source(s) of this degradation.

4.4.5 Copper Deposition and Patterning

Copper deposition was originally intended to be performed externally; however, due to equipment limitations this was not possible. As discussed in the Chapter 3, difficulties were experience with copper lithography and liftoff, causing the device wafers to be exposed to developer multiple times. This is believed to be one of the main factors leading to the high series resistances observed. Additionally, the limitations of this non-optimized process may have induced uncertainty in the TLM dimensions, contributing to error.

The difference in contact resistance between the NiSi and NiSi/Cu/TiN was likely impacted by these process non-idealities. Without Cu/TiN, a contact resistance range of $7.3 \times 10^{-6}\,\Omega\,\mathrm{cm}^2$ to $1.5 \times 10^{-4}\,\Omega\,\mathrm{cm}^2$ was measured. With Cu/TiN, a range of $4.0 \times 10^{-5}\,\Omega\,\mathrm{cm}^2$ to $2.7 \times 10^{-4}\,\Omega\,\mathrm{cm}^2$ was measured.

4.4.6 Adequacy of TiN Capping Layer

Further studies using this process will require an adequate Cu oxidation barrier. This was not characterized in this work. Increasing the thickness of this layer may prove effective, however it is important that the resistivity of this film be further characterized so as not to add resistance to the cell.

4.5 Passivated Tunneling Contacts for High Efficiency Cells

4.5.1 Contact Resistivity

The contact resistance of 28.5 nm NiSi passivated contacts, without an a-Si cap, was measured for both n and p-type substrates. The contact showed low resistance,

greater than $10\,\mathrm{m\Omega\,cm^{-2}}$ in only one case. Table 4.4 summarizes these results.

Substrate Doping	$\boldsymbol{\rho_c}$ ($\mathrm{m\Omega\,cm^{-2}}$)	$\boldsymbol{\rho_c, \rho_m}$ **included** ($\mathrm{m\Omega\,cm^{-2}}$)	$\boldsymbol{\rho_s}$ ($\mathrm{m\Omega\,cm^{-2}}$)
Phosphorus	1.8	0.98	102
Phosphorus	5.0	3.7	94.3
Phosphorus	6.8	5.5	105
Phosphorus	8.1	6.8	46.9
Phosphorus	44	50	36.6
Boron	4.1	3.1	175
Boron	4.9	3.9	229
Boron	8.3	7.0	165

Table 4.4: TLM Measurement of NiSi metallized tunneling contact.

Contact resistance was also measured on n-type substrates with the additional a-Si cap. This resulted in a best contact resistivity of $1.8 \times 10^{-3}\,\mathrm{m\Omega\,cm^{-2}}$. The contact resistivity of these samples is shown as a function of NiSi thickness in Figure 4.12. There may be a slight increase in contact resistance with thinner NiSi. This follows the same trend observed for the RIT fabricated solar cells. More data collection is needed to determine if this trend holds up to a more statistically relevant sample size. It should be noted that the contact resistivity of the tunneling contact with the a-Si cap is in the same $1.8\,\mathrm{m\Omega\,cm^{-2}}$ to $8.1\,\mathrm{m\Omega\,cm^{-2}}$ range as the contacts without the cap.

The a-Si and poly-Si thicknesses could be optimized in future studies by further characterizing the Ni/a-Si silicidation. The two-step Ni silicidation process may provide the enhanced process control needed in this particular application.

4.5.2 Photoluminescence (PL) and Implied V_{oc}

Photoluminescence was measured through the rear of the samples to avoid blocking the emitted light. The samples were oriented as shown in the insert of Figure 4.10. The PL of an a-Si:P/poly-Si:P/SiO_2/c-Si tunneling contact both with and without

NiSi is shown in Figure 4.10. This is a marked improvement from the original attempt at producing such contacts, as shown in Figure 4.11. The addition of the a-Si cap and reduction in NiSi thickness can be credited with the improvement.

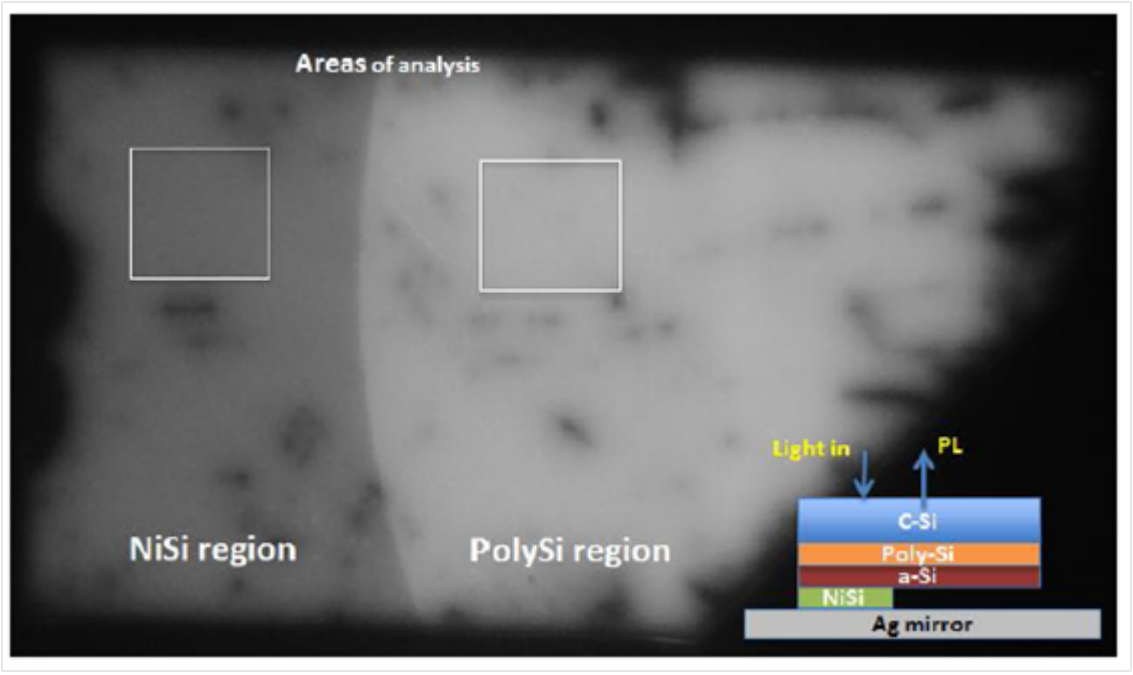


Figure 4.10: The photoluminescence of a tunneling contact with and without NiSi.

The sample on the right in Figure 4.11 has NiSi TLM structures. The sample on the left has similar TLM structures, however Ni/Al was used as the metal. The PL from the Ni/Al contacts actually showed *improved* passivation at the contacts as compared to the bulk material, whereas the NiSi contacts show significant degradation in passivation.

The PL intensity was averaged over an area, like that shown in Figure 4.10. This intensity was used to calculate the drop in iV_{oc} per Equation 2.14. The result of this analysis on unpatterned, blanket a-Si:P/poly-Si:P/SiO_2/c-Si contacts is shown

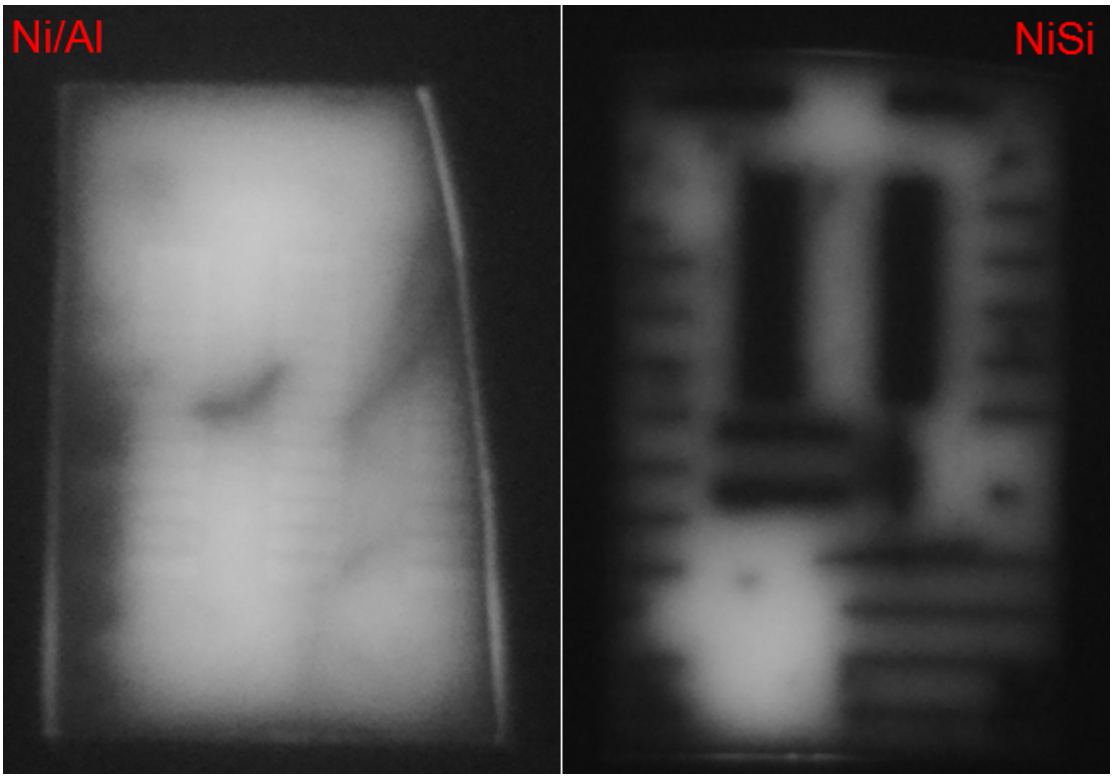


Figure 4.11: The photoluminescence of a tunneling contact with and without NiSi.

in Figure 4.12.

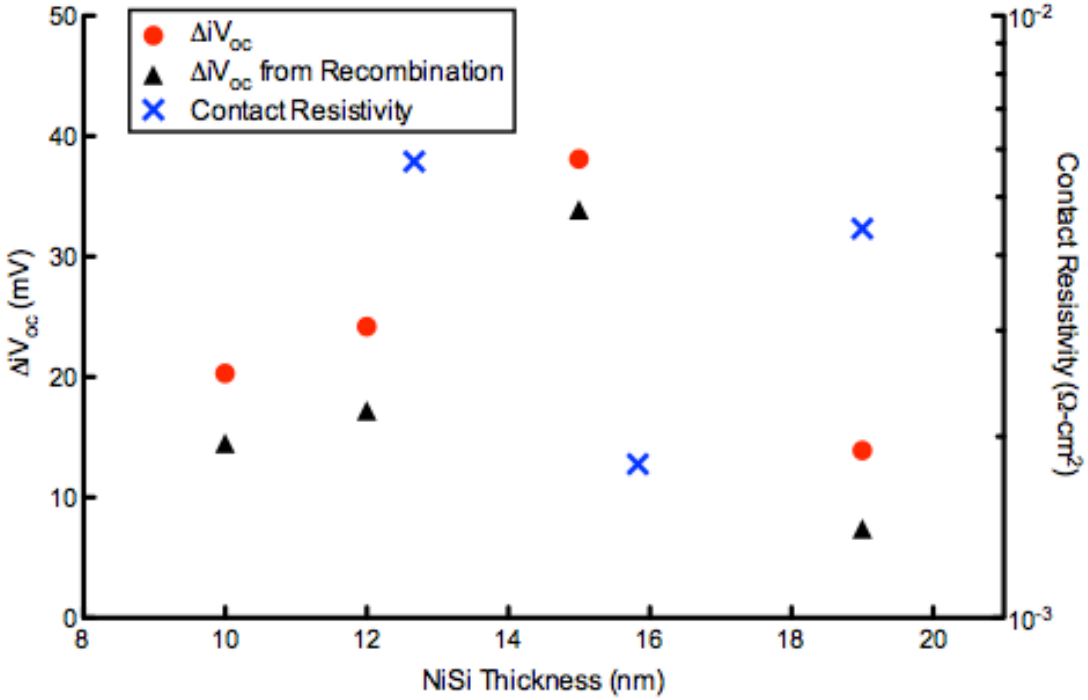


Figure 4.12: The results of contact resistivity and ΔiV_{oc} measurements on passivated tunnelling contacts with varying thicknesses of NiSi

Rear Internal Reflectance

Since these contacts are used on the back of the wafer, light passes through the entire solar cell before it reaches them. The only light that hasn't been significantly reduced in intensity due to absorption at this depth in the cell is longer wavelength light. It is desirable to have an internally reflective back surface so that the long wavelength light that reaches this depth can be reflected back into the cell, increasing the probability of absorption.

Reflectance was measured using the setup shown in the insert of Figure 4.13. There was a strong difference in reflectance at wavelengths greater than 950 nm due

to absorption in the NiSi. This optical effect can be calculated based on the difference in reflectance, much like in Equation 2.15. The difference in reflectance for the 12 nm NiSi sample at the silicon band gap energy is shown in Figure 4.13. This value was used to calculate a drop in iV_{oc} of 8 mV due to optical absorption of the PL signal in the NiSi. This was done for all samples individually but these are not shown in Figure 4.13 for simplicity. The corrected drop in iV_{oc} is shown in Figure 4.12. This is due only to recombination. For the 12 nm sample the drop in iV_{oc} from recombination is therefore 16 mV, down from a total of 24 mV including optical effects. Since iV_{oc} in the range of 730 mV have been realized using these methods on non-metallized contacts[31], it can be concluded that an iV_{oc} greater than 700 mV is possible.

The recombination loss appears to scale linearly with thickness. This likely means the passivation quality of the oxide has been damaged by the silicidation. Further characterization of the Ni/a-Si silicidation process will likely yield improvements in this regard. Nonetheless this shows the potential value of using the two step silicidation process where more precision can be maintained. The apparent improvement in the passivation of the 19 nm NiSi appears to be an anomaly. Future experimentation will test the legitimacy of this data point.

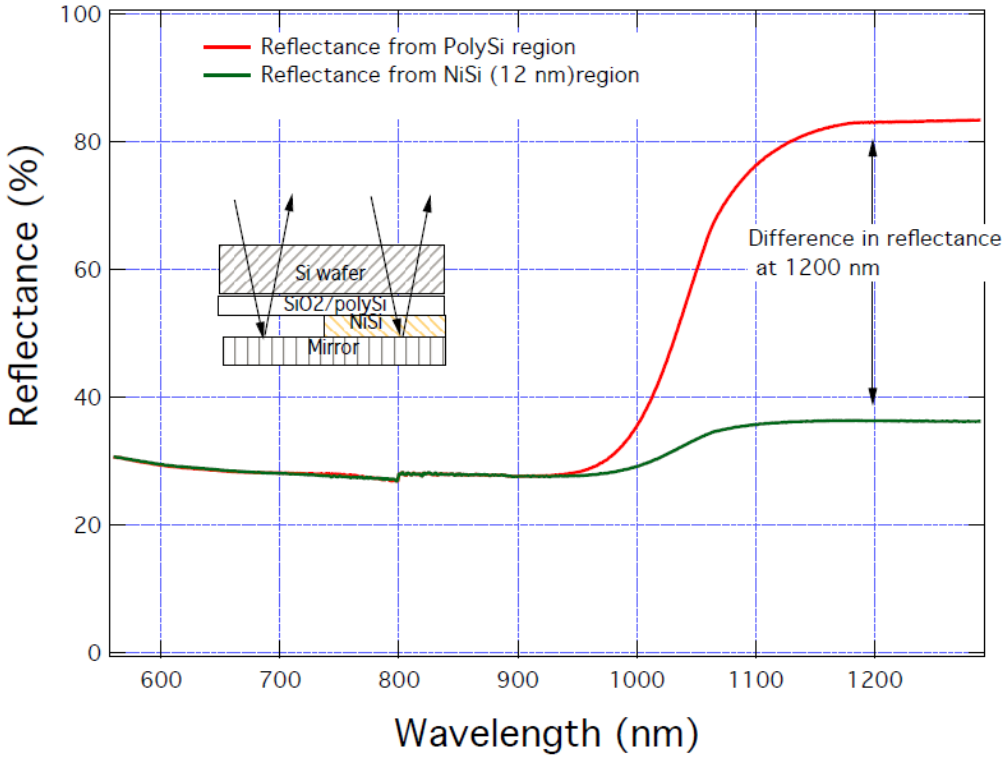


Figure 4.13: Reflectance of NiSi compared to poly-Si

Chapter 5

Conclusions

Nickel monosilicide (NiSi) has shown to be a viable contact material for silicon solar cells. This was evaluated on fully processed solar cell device wafers. Contact resistance was evaluated for NiSi both with and without Cu/TiN metallization using the Transmission Length Method (TLM). Best contact resistivities of $7.3 \times 10^{-6}\,\Omega\,\mathrm{cm}^2$ with NiSi only and $4.0 \times 10^{-5}\,\Omega\,\mathrm{cm}^2$ with NiSi/Cu/TiN were measured. Even following a week of temperature stress, NiSi maintained solar cell performance parameters such as pseudo fill factor (pFF) and quantum efficiency (QE) better than Cu/TiN contacts without NiSi and at least as good as Ti/Pd/Ag contacts on average. The solar cells' performance show there are significant issues with both series resistance and minority carrier lifetime. Suns-V_{oc} and AM1.5 I-V measurements estimate a total series resistance between $0.89\,\Omega\,\mathrm{cm}^2$ to $2.06\,\Omega\,\mathrm{cm}^2$. PC1D matching of QE measurements estimate a minority carrier lifetime of $2.8\,\mu\mathrm{s}$. This is hypothesized to be the cause of poor resolution in the suns-V_{oc} degradation metric, pFF.

This characterization effort was extended to examine high efficiency, textured, passivated, tunneling contact solar cells. Devices were fabricated in cooperation with the National Renewable Energy Laboratory. TLM, photoluminescence (PL) implied open circuit voltage δiV_{oc} and optical measurements were used. It can be concluded

from this work that a cell capable of an open cicuit voltage near 700 mV could be produced using such a contact scheme, although NiSi was shown to degrade the passivation quality of the tunneling contact.[22] Contact resistances below 2 $m\Omega\,cm^2$ were formed despite the Ni/a-Si silicidation process remaining imperfect, especially on a textured surface.

5.1 Papers Published During This Thesis Research

1. A. Marshall, K. Florent, A. Tapriya, B. G. Lee, S. K. Kurinec and D. L. Young, "Nickel silicide metallization for passivated tunneling contacts for silicon solar cells," 2016 IEEE 43rd Photovoltaic Specialists Conference (PVSC), Portland, OR, 2016, pp. 2479-2482. doi: 10.1109/PVSC.2016.7750089

2. A. Kale et al., "Study of nickel silicide as a copper diffusion barrier in monocrystalline silicon solar cells," 2016 IEEE 43rd Photovoltaic Specialists Conference (PVSC), Portland, OR, 2016, pp. 2913-2916. doi: 10.1109/PVSC.2016.7750190

References

[1] *Global Market Outlook for Photovoltaics 2014-2018*, 2014.

[2] *GTM Research/SEIA: U.S. Solar Market Insight: Q3 2014*, 2014.

[3] *Photovoltaic System Pricing Trends*, 2014.

[4] *Key Issues and Innovations in Photovoltaic Metallization*, 2012.

[5] *International Technology Roadmap for Photovoltaics: Fifth Edition*, 2017.

[6] M. R. et al., "Review of Ni-Cu based front side metallization for c-Si solar cells," *Journal of Solar Energy*, vol. 2013, 2013.

[7] *Fraunhofer ISE: Photovoltaics Report*, 2014.

[8] "InfoMine, Available: www.infomine.com, Accessed: 2017-05-01."

[9] *Copper as conducting layer in advanced front side metallization processes for crystalline silicon solar cells, exceeding 20% on printed seed layers.*, no. 35th IEEE, Photovoltaic Specialists Conference (PVSC). IEEE, 2010.

[10] D. Fisher, *Diffusion in Silicon: 10 Years of Research.* Scitec Publications Ltd., 1998.

[11] M. Bohra, "Process development for single-crystal silicon solar cells," Master's thesis, Rochester Institute of Technology, 2014.

[12] K. Duggimpudi, "Characterization of grid contacts for n-si emitter solar cells," Master's thesis, Rochester Institute of Technology, 2016.

[13] "PV Education, Available: www.pveducation.org, Accessed: 2017-05-01."

[14] A. D. et al., "Teaching solar cell i-v characterisics using spice," *American Journal of Physics*, vol. 79, 2011.

[15] A. Richter, "Improved parameterization of auger recombination in silicon," *Energy Procedia*, vol. 2, 2012.

[16] S. S. et al., *Physics of semiconductor devices.* John Wiley and Sons, 2006.

[17] Y. Tao, "Screen printed front junction n type silicon solar cells," in *Printed Electronics - Current Trends and Applications*, I. Yun, Ed. Rijeka: InTech, 2016, ch. 04. [Online]. Available: http://dx.doi.org/10.5772/63198

[18] *Semiconductor Material and Device Characterization.* Wiley Interscience, 1976.

[19] D. K. S. et al., "Solar cell contact resistance-a review," *IEEE Transactions on Electron Devices*, 1984.

[20] "Princeton Instruments, Available: www.princetoninstruments.com, Accessed: 2017-05-01."

[21] R. Sinton, "Contactless determination of current–voltage characteristics and minority-carrier lifetimes in semiconductors from quasi-steady-state photoconductance data," *Applied Physics Letters*, vol. 69, no. 17, pp. 2510–2512, 1996. [Online]. Available: http://link.aip.org/link/?APL/69/2510/1

[22] A. M. et al., "Nickel silicide metallization for passivated tunneling contacts for silicon solar cells," in *2016 IEEE 43rd Photovoltaic Specialists Conference (PVSC)*, June 2016, pp. 2479–2482.

[23] M. Yasaka, "X-Ray thin film measurement techniques," *The Rigaku Journal*, vol. 26, 2010.

[24] M. A. et al., "Advances in electroless nickel plating for the metallization of silicon solar cells using different structuring techniques for the ARC," in *24th Eurpoean PV Solar Energy Conference and Exhibition*, 2009.

[25] D. S. K. et al., "Low-cost contact formation of high-efficiency crystalline silicon solar cells by plating," *Journal of the Korean Physical Society*, 2005.

[26] K. Fisher, "The pitfalls of pit contacts: Electroless metallization for c-si solar cells," Ph.D. dissertation, University of New South Wales, 2004.

[27] H. I. et al., "NiSi salicide technology for scaled cmos," *Microelectronic Engineering*, 2002.

[28] *Silicide Technology for Integreated Circuits.* The Institution of Engineering and Technology, 2004.

[29] P. S. et al., Ed., *Binary alloy phase diagrams.* American Sciety for Metals, 1986, vol. 1, no. 2.

[30] J. F. et al., "Optimizing the formation of nickel silicide," *Materials Science and Engineering*, 2004.

[31] *Low temperature SiSiOxpci passivated contacts to n-type Si solar cells*, no. 40, Photovoltaic Specialists Conference (PVSC). IEEE, 2014.

[32] C. R. et al., "Tunnel oxide passivated contacts formed by ion implantation for applications in silicon solar cells," *Journal of Applied Physics*, vol. 118, 2015.

[33] *Passivated tunnelling contacts to n-type wafer silicon and their implementation into high performance solar cells*, no. 6, World Conference on Photovoltaic Energy Conversion. NREL, 2014.

[34] *Nickel silicide metallization for passivated tunneling contacts for silicon solar cells*, no. 43, Photovoltaic Specialists Conference (PVSC). IEEE, 2016.

[35] *Utilization of Tabula Rasa to stabilize bulk lifetimes in n-Cz silicon for high-performance solar cell processing*, no. 43, Photovoltaic Specialists Conference (PVSC). IEEE, 2016.

[36] H. U. et al., "Error analysis leading to design criteria for transmission line model characterization of ohmic contacts," *Electron Devices*, vol. 48, 2001.

[37] A. G. et al., *Crystalline silicon solar cells*. John Wiley & Sons Ltd Sons Ltd, 1998.

[38] J. D. J. et al., "Impurities in silicon solar cells," *IEEE Transactions on Electron Devices*, vol. ED-27, no. 4, pp. 677–687, April 1980.

[39] *International Technology Roadmap for Photovoltaics: Eighth Edition*, 2014.

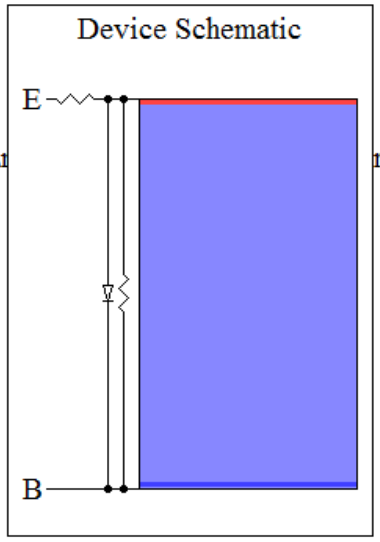
[40] *Study of nickel silicide as a copper diffusion barrier in monocrystalline silicon solar cells*, no. 43, Photovoltaic Specialists Conference (PVSC). IEEE, 2016.

[41] C. B. et al., "Photoluminescence image evaluation of solar cells based on implied voltage distribution," *Solar Energy Materials & Solar Cells*, vol. 128, 2014.

Appendix A

PC1D Input File

DEVICE
Device area: 1 cm^2
No surface texturing
No surface charge
Front reflectance from c:\users\w0017686\desktop\r_c18.ref
No Exterior Rear Reflectance
Internal optical reflectance enabled
  Rear surface optically rough
Emitter contact: 0.0204082 Ω
Base contact enabled
Internal diode: 7.693×10^{-7} A
Internal conductor: 3.0625×10^{-4} S



REGION 1
Thickness: 525 µm
Material modified from program defaults
  Carrier mobilities from internal model
  Dielectric constant: 11.9
  Band gap: 1.124 eV
  Intrinsic conc. at 300 K: 1×10^{10} cm^{-3}
  Refractive index from si.inr
  Absorption coeff. from si300.abs
  Free carrier absorption enabled
P-type background doping: 4.72×10^{15} cm^{-3}
  1st front diff.: N-type, 2.336×10^{19} cm^{-3} peak
  No 2nd front diffusion
  1st rear diff.: P-type, 3.648×10^{19} cm^{-3} peak
  No 2nd rear diffusion
Bulk recombination: $\tau_n = \tau_p = 2.8$ µs
  Front-surface recom.: S model, $S_n = S_p = 3\times10^5$ cm/s
  Rear-surface recom.: S model, $S_n = S_p = 1\times10^{20}$ cm/s

Appendix B

Athena Input Files

B.1 Emitter

```
go athena


line x loc=0 spac=0.1

line x loc=0.35 spac=0.02

line x loc=0.6 spac=0.1


line y loc=0.00 spac=0.005

line y loc=0.3 spac=0.015

line y loc=0.5 spac=0.02

line y loc=2 spac=0.2

line y loc=5 spac=1


init orientation=100 boron resistivity=2 space.mult=2

#RCA clean

#grow oxide or

#depo oxide thick=0.1
```

#Recipe 311, Tube 1

diffus time=12 temp=800 nitro

diffus time=10 temp=800 t.final=900 nitro

diffus time=5 temp=900 dryo2

diffus time=45 temp=900 weto2

diffus time=12 temp=800 nitro

diffus time=5 temp=900 t.final=25 nitro

#tonyplot

#extract oxide thickness

extract name="Oxide1" thickness material="SiO 2" mat.occno=1 x.val=0.4

#etch oxide off back

#Remove PR from front

#etch oxide all

#Marshall BSF predep

#Recipe 211, Tube 2

diffus time=12 temp=800 nitro

diffus time=20 temp=800 t.final=1000 nitro

diffus time=15 temp=1050 nitro

diffus time=3 temp=1050 dryo2

diffus time=5 temp=1050 weto2

diffus time=3 temp=1050 dryo2

diffus time=30 temp=1000 t.final=25 nitro

tonyplot

#extract oxide thickness

extract name="Oxidepredepplusscreen" thickness material="SiO 2" mat.occno=1 x.val=0.4

#remove skin

#etch oxide from both sides

etch oxide all

#BSF drive in

#Recipe 143, Tube 1,2,3

diffus time=12 temp=800 nitro

diffus time=30 temp=800 t.final=1100 dryo2

diffus time=45 temp=1100 nitro

diffus time=15 temp=1100 t.final=1000 nitro

diffus time=10 temp=1000 weto2

#8min weto2, for correct tox

diffus time=5 temp=1000 nitro

diffus time=60 temp=1000 t.final=25 nitro

#tonyplot

#extract oxide thickness

extract name="OxideBSFDrivein" thickness material="SiO 2" mat.occno=1 x.val=0.4

#implant front

implant phosphorus dose=8e14 energy=120 pearson

tonyplot

#emitter drive in

Recipe 145, 20min soak

diffus time=15 temp=800 nitro

diffus time=20 temp=800 t.final=1000 nitro

diffus time=20 temp=1000 nitro

diffus time=40 temp=1000 t.final=600 nitro

#tonyplot

etch oxide all

```
tonyplot

extract name="xjemitter" xj material="Silicon" mat.occno=1 x.val=0 junc.occno=1

extract name="rho" sheet.res material="Silicon" mat.occno=1 x.val=0 region.occno=1

quit
```

B.2 Back Surface Field

```
go athena

line x loc=0 spac=0.1

line x loc=0.35 spac=0.02

line x loc=0.6 spac=0.1

line y loc=0.00 spac=0.005

line y loc=0.3 spac=0.015

line y loc=0.5 spac=0.02

line y loc=2 spac=0.2

line y loc=5 spac=1

init orientation=100 boron resistivity=2 space.mult=2

#RCA clean
```

```
#grow oxide or

#depo oxide thick=0.1

#Recipe 311, Tube 1

diffus time=12 temp=800 nitro

diffus time=10 temp=800 t.final=900 nitro

diffus time=5 temp=900 dryo2

diffus time=45 temp=900 weto2

diffus time=12 temp=800 nitro

diffus time=5 temp=900 t.final=25 nitro


#tonyplot


#extract oxide thickness

extract name="Oxide1" thickness material="SiO 2" mat.occno=1 x.val=0.4


#etch oxide off back

#Remove PR from front

etch oxide all


#predep

#Recipe 110, Tube 2

diffus time=12 temp=800 nitro

diffus time=20 temp=800 t.final=1000 nitro c.boron=2e20
```

diffus time=10 temp=1050 nitro c.boron=2e20

diffus time=10 temp=1050 weto2 c.boron=2e20

diffus time=30 temp=1000 t.final=25 nitro

tonyplot

#extract oxide thickness

extract name="Oxidepredep" thickness material="SiO 2" mat.occno=1 x.val=0.4

#remove skin

#etch oxide from both sides

etch oxide all

#BSF drive in

#Recipe 143, Tube 1,2,3

diffus time=12 temp=800 nitro

diffus time=30 temp=800 t.final=1100 dryo2

diffus time=50 temp=1100 nitro

diffus time=15 temp=1100 t.final=1000 nitro

diffus time=10 temp=1000 weto2

diffus time=5 temp=1000 nitro

diffus time=60 temp=1000 t.final=25 nitro

```
#tonyplot

#extract oxide thickness

extract name="OxideBSFDrivein" thickness material="SiO 2" mat.occno=1 x.val=0.4

#implant front

#emitter drive in

diffus time=15 temp=800 nitro

diffus time=20 temp=800 t.final=1000 nitro

diffus time=20 temp=1000 nitro

diffus time=40 temp=1000 t.final=600 nitro

#tonyplot

etch oxide all

tonyplot

#extract name="xjback" xj material="Silicon" mat.occno=1 x.val=0 junc.occno=1

extract name="rho" sheet.res material="Silicon" mat.occno=1 x.val=0 region.occno=1

quit
```